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# Epileptic Seizure Prediction Using Fully Integrated Neural Signal Acquisition Amplifier

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***Abstract*: This paper deals with the design of low power low noise neural signal amplifier for Epileptic Seizure Prediction. The advent of Micro-electro Arrays has driven the need for implantable electronic circuitry to detect those Extracellular neural signals (ENG). We proposed a preamplifier of fully differential Low Noise Amplifier (LNA) with gm boosting in order to enhance the gain as well as reduce the power consumption. Low frequency high pass function has been realized with anti-parallel Diode connected PMOS. Simulation results shows that the input referred noise is 1.24µVrms from 100Hz to 5 KHz, mid-band voltage gain of 44.6dB, and the power consumption is 18.74µw. A new signal processing circuit has been designed extract the seizure onset. The results are validated using Cadence spectre simulator with 180nm technology. Simulation results show that this implantable amplifier is suitable for Epileptic seizure prediction.**

***Keywords*: Epileptic Seizure, NSA, pseudo resistor, Low frequency High Pass Function (LFHPF)**

## 1. Introduction

Early prediction of severe epilepsy may helpful for the patients to escape from fatal accidents. Much research is being done on Epileptic seizure prediction using EEG Signals. While using EEG signals many false positives are reported. So, the better alternate for this system is to use implantable devices recording ENG signals. ENG signals are small in amplitude from 5µV to 500µV and have a low frequency spectrum of 100Hz to 5 KHz [1]. However in practice, the distance of Micro-electrode arrays (MEA) are difficult to control and the resulting ENG is very small requiring a LNA for signal amplification cum detection. The overall block diagram for Epileptic Seizure detection is shown in figure1. Output from the ENG signal acquisition amplifier (NSA) is directly taken as clinical data, further the signal is sent through a proposed simple signal processor to extract the seizure onset. Later the extracted feature will be compared with the reference neural signal Potential (Vsyn) using high speed latch comparator. [2]. The composite Neural signal consists of large DC offset due to the body fluid where the MEA resides and Electromyography (EMG) noise, Power Line frequency interference. The DC offset and EMG noise can be removed by Low frequency High Pass Function [3]. MOSFET based design for low frequency bio-medical application has inherent flicker noise, it cause poor SNR. Some of the solutions to reduce the flicker noise are chopper stabilization and Auto-zeroing, both cases consumes more power, it is not advisable for implantable applications [4], [5]. The flicker noise is dominating in the PMOS. The flicker noise and the valid signals are having the same 150Hz spectrum, so the transistors made large to increase its trans conductance (gm) [6], thereby the noise is eliminated. The proposed LNA with sub-threshold PMOS input pair with gm-boosting shows valid results

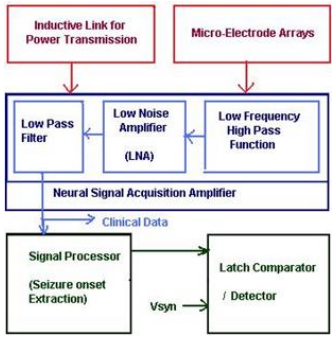

Fig. 1. Overall Block Diagram of Epileptic Seizure Detection

This LNA has fully differential topology in order to eliminate the coherent noise. The design of low frequency High pass function is challenging one. In our proposed Circuit Anti-parallel Diode connected PMOS is used as Pseudo resistor. It consumes less power and exhibits bilinear characteristics. The differential output is converted into single ended by the high linear OTA-C filter, which is nothing but a Low pass Filter in this design [6]. The section1 gives brief Introduction of this Work, section II explain the inductively coupled power supply for implantable circuits, section III explains the realization of Pseudo-resistors, section IV describes the functionality of low frequency high pass function, section V explains the functional details of LNA, Section VI reveals the LNA Noise Analysis, Section VII explains about the High Linear Low Pass filter, section VIII explains a new signal processing circuit and Section IX Concludes the work with the obtained parameters.

## 2. Inductive coupled rail-to-rail supply

For the past few years, high-performance implantable bio-medical ICs plays a major role in modern medicine. With the advent of nanotechnology, Battery based circuits are not entertained for implantable applications. Nowadays, inductively coupled link is more desirable method for patient,

because of its high power transfer efficiency and safety. Bio-medical amplifiers shows good result, when using rail-to-rail power supply. In the proposed method, the sinusoidal output from the secondary coil is applied between the terminals X and Y. When potential on side X is more than that of Y, the transistors Mb,Mc,Mf and Mg are forces to shut-off while Ma,Md,Me and Mh are turned on. Therefore, we can get positively and negatively unidirected supply from terminals +Vr and –Vr respectively for both positive and negative half cycles. The unidirected supply is passed through a capacitor filter to remove its ac contents (ripples). By using a suitable regulator we can a dc for the circuit. For the regulation, zener diode is not preferred because of its parasitic capacitance. Some CMOS circuits based on voltage reference may be use

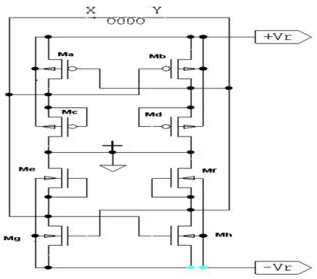


Fig. 2(a) Rail-to-Rail Rectifier Circuit

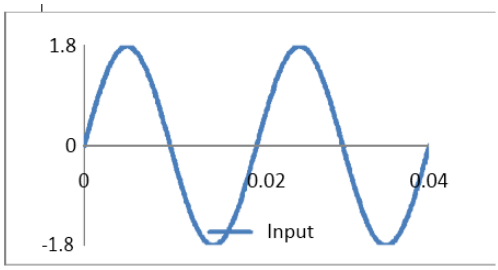


Fig. 2(b) Output waveform

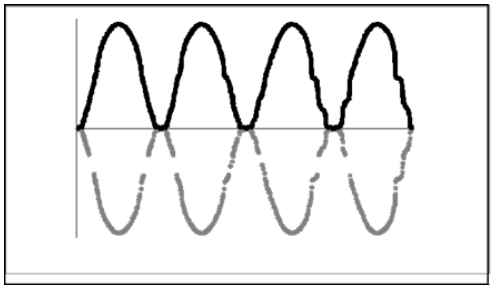

Fig. 2(c) Output waveform

### 3. Pseudo-resistors

The Pseudo-resistors plays a vital role in the realization of low frequency high pass function, in order to avoid large on-chip capacitor resulting high power consumption and poor SNR, The resistors of the order of several Giga- ohms are needed for this circuit [7]. There are six different structures as shown in the figure3.The linear variation of current for each structure is plotted for comparison. The Fig 3(a) and 3(b) shows the uni-linear, resulting noise disturbance is more.

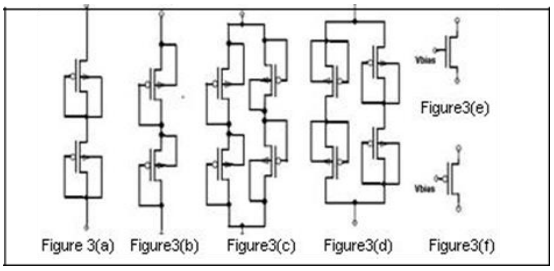


Fig. 3. Different Structures of Pseudo-Resistor

The transfer characteristics for single and anti-parallel connected is shown in the figure 4. From this I-V curve we can understand the anti-parallel connected (DoubDio & DoubSG) pseudo resistor exhibits bilinear characteristics. The Fig. 3, uses sub-threshold PMOS and deep-depletion NMOS respectively. In both cases, it needs additional biasing for tuning purpose. For implantable applications, the supply is applied externally through inductive coupling. Therefore the design with large number of biasing is not preferred. The Fig. 4, shows bilinear characteristics and doesn't require additional biasing for tuning purpose. Out of these two, Fig. 3 is better suited for this application due to high linearity. The linear resistance curve is shown in figure5

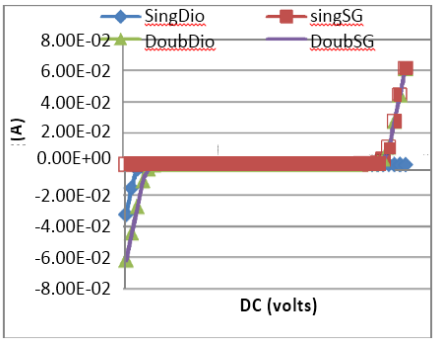


Fig. 4. Transfer characteristics of pseudo-resistors

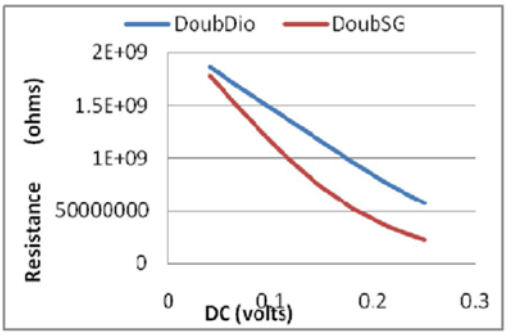


Fig. 5. Linearity Comparison of Anti-parallel Diode connected and Source-Gate connected

The drain current of PMOS transistor operating in sub-threshold region is

$$I_d = I_o\left[1 - exp\left(\frac{V_d}{V_t}\right)\right]\exp\left[\frac{V_g - V_{th} - V_{eff}}{nV_t}\right] \quad (1)$$

Where, $I_d$ = drain Current; $V_d$ = source- drain voltage; $V_t$ = thermal voltage; $V_{th}$ = threshold voltage; n = sub-threshold swing parameter; $V_g$ = gate-source voltage.

The differential resistance ∂R can be obtained by differentiating $I_d$ with respect to $V_d$.

$$\frac{\partial I_d}{\partial V_d} = \frac{1}{R_{out}} = \frac{I_o}{V_t}.\exp\left[\frac{V_g - V_{th} - V_{eff}}{nV_t}\right].exp\left(\frac{V_d}{V_t}\right) \quad (2)$$

### 4. Low frequency high pass function

This circuit serves two purposes. First, it avoids the DC voltage value of the body fluid where the MEAs are placed, because Dc voltage may saturate the output of LNA. Second, it removes the EMG noise spectrum which resides within 100Hz. This circuit is built by the pseudo-resistors, in order to avoid the high power consumption. The mid-band gain value is set by the capacitors C1 and C2 [8]. For bio-medical implantable applications, mid band- gain normally chosen by the ratio of c1 and c2 as 50. We can use either open loop or closed loop configuration as shown in Fig. 6.

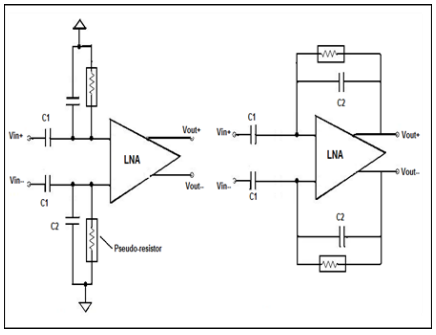


Fig. 6. Open Loop and Closed Loop Configuration

Simulation results show that the open loop configuration is better due to the high gain and Low Power consumption. No stability problem arises around the region of interest.

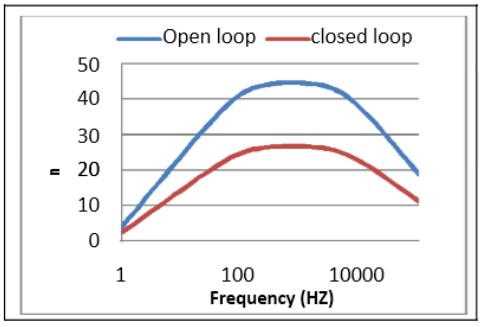


Fig. 7. Gain Comparison between open loop and closed loop configuration

### 5. Low noise amplifier (LNA)

Fig. 8 shows the fully differential LNA circuit. Two sub-threshold PMOS input transistor pair M1 and M2 plays a vital role to reduce the flicker (1/f) noise in the circuit, because it cannot be eliminated in the succeeding stages[10]. Most of the designers prefer PMOS than NMOS; the reason behind this is NMOS gives more gain and more noise. To reduce the flicker noise, we have to choose the trans conductance gm1 >> gm3 > gm5 by changing W/L ratio. To increase the trans conductance of the input transistor, we use gm-boosting method to steer the current into the modified active load. The trans conductance can be varied by changing the W/L ratio of the M5, M7. The above said condition also applicable to the negative counterpart of the amplifier. This proposed method of active load increases the gain of the amplifier with low power consumption. The transistors M20, M21and M22 provide the biasing to LNA.

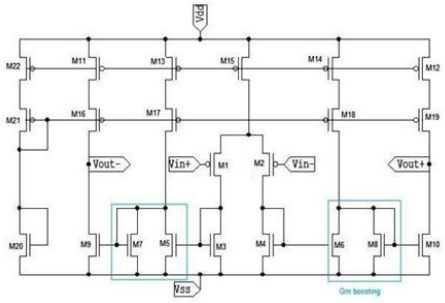


Fig. 8. LNA circuit diagram

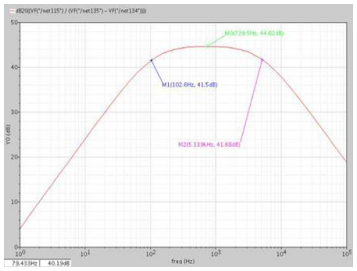

Fig. 9. Gain Plot of LNA amplifier

### 6. LNA noise analysis

Channel thermal noise of a MOSFET is derived from the noise current equation.

$$i_{n^2} = 4.\gamma.k.T.g_m \quad (3)$$

Where, k – Boltzmann Constant; T – Absolute Temperature; = trans conductance.

The factor is a complex function of the basic transistor parameters and bias conditions. For modern CMOS processes with oxide thickness

in the order of 50nm and with a lower substrate doping Nb of about $10^{15} – 10^{16}$ $cm^{-3}$, the factor

is between 0.67 and 1[9].

$$v^2_{n,input} = \frac{8\,kT\gamma}{g_{m1}}\left[1 + 2.\frac{g_{m10}}{g_{m1}}\frac{g_{m6}}{g_{m8}} + \frac{g_{m12}}{g_{m1}}\right] \quad (4)$$

Therefore, to reduce input-referred thermal noise, the W/L ratios of M1&M2 and the lengths of M1 & M2 are chosen to be very large, thereby maximizing the trans conductance of M1 & M2, while minimizing those of M9 and M10. The input devices

are the primary source f flicker noise; therefore large area PMOS transistors are used.

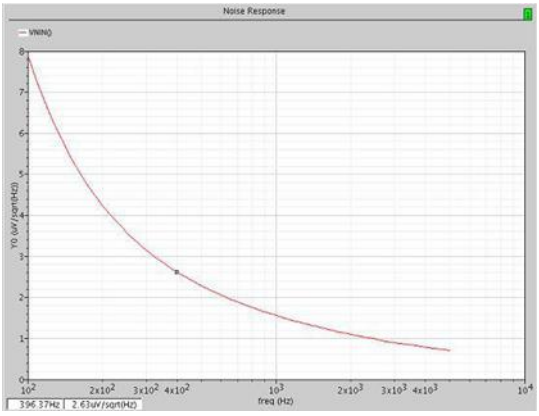


Fig. 10. Input referred Noise Response

### 7. Low pass filter

High linear, OTA-C filter based simple Low pass filter is shown in the figure10. Linearity of the low pass filter is improved by source degeneration topology. In this circuit the transistors biased on triode region. M25-M26 work in a saturation-active mode for positive Vin in an active-saturation mode for negative Vin, Can result in a linear operation. The linear range is limited to $V_{in} < V_{Dsat}$.

The trans conductance value for this low pass filter can be calculated from the equation given below.

$$g_m \approx \frac{g_{m27}}{1+\frac{\beta_{29}}{4\beta_{23}}} \quad (5)$$

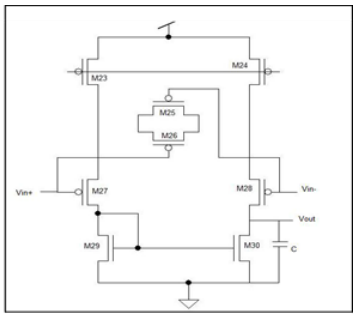


Fig. 11. High Linear Low Pass Filter.

### 8. The bulk driven signal processor

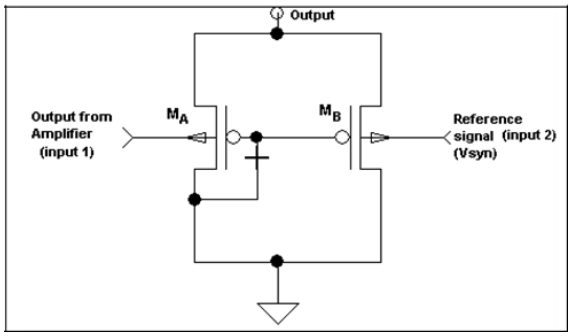


Fig. 12. A new Signal processing unit

For implantable bio-medical applications, gate-driven MOSFET posing threshold voltage constraint. A new processor using bulk-driven MOSFET has been developed to handle very small signals in the range of several millivolts. Both, bulk-driven and gate-driven performances are same except the physical size of former is small. The first order equation shows the VBS and its effect on drain current.

$$i_D = K\left(V_{GS} - V_T - \frac{\eta}{2}V_{DS}\right)\cdot V_{DS} \quad \ldots\ldots V_{DS} \le V_{DS,sat}$$

$$i_D = K(V_{GS} - V_T)^2 \cdot (1 + \lambda . V_{DS}) \quad \ldots\ldots V_{DS} \ge V_{DS,sat}$$

$$\text{Where, } \eta = 1 - \frac{\gamma}{2\sqrt{\phi_j - V_{BS}}} \quad ; \quad V_{DS,sat} = \frac{V_{GS}-V_T}{\eta}$$

$$V_T = V_{T0} - \gamma\sqrt{2\phi_F - V_{BS}} + \gamma\sqrt{2\phi_F}$$

The seizure onset from the neural signal can be clipped-off by the processor. Later, it compared with the reference signal using high speed latch comparator. Thereby, seizure onset can be detected.

The circuit used to extract the seizure onset is shown in the Fig. 12. Neural signal from the amplifier is applied at the bulk of transistor $M_A$. Here, Gate and source is tied to make $V_{GS}$ constant. Therefore, the output variation is only due to bulk potential. When input is greater than zero, inverse depletion layer is formed and it causes current to flow through the transistor $M_A$. The neural reference potential $V_{SYN}$ for the normal behaviour is applied to the bulk of $M_B$.

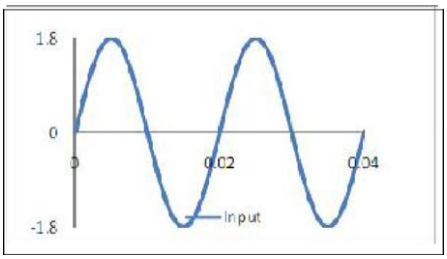


Fig. 13. Sample Input waveform

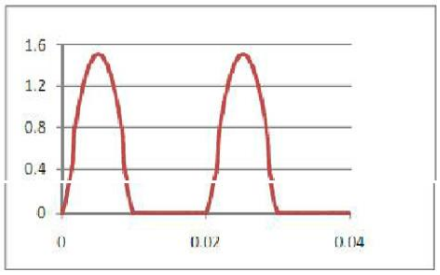


Fig. 14. Output waveform when $V_{syn}$ = 0 V

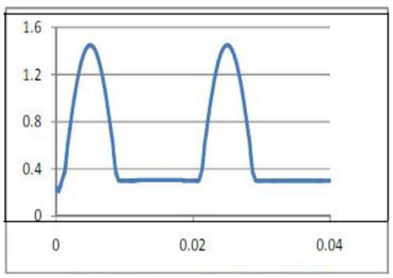


Fig. 15. Output waveform with $V_{syn}$ =0.3 V

Table 1
Device sizing
*Length of all transistors = 0.18µm*

| ***Devices*** | ***Width (µm)*** | ***Devices*** | ***Width (µm)*** |
|---|---|---|---|
| M1, M2 | 10 | M20 | 0.24 |
| M3,M4 | 2 | M21,M22,M23 | 2 |
| M5,M6 | 8 | M24,M27,M28 | 2 |
| M7,M8,M9,M10 | 2 | M29,M30 | 0.5 |
| M11,M12,M13 | 2 | For Pseudo resistors | 5 |
| M14,M15,M16 | 2 | | |
| M17,M18,M19 | 2 | | |

Table 2
Simulated parameters

| **S.No.** | **Specification** | **Values** |
|---|---|---|
| **1** | Over-all Gain | 44.6 dB |
| **2** | LFHPF cut-off Frequency | 100Hz |
| **3** | LPF Cut-off frequency | 5 KHz |
| **4** | CMRR | 68dB |
| **5** | Input referred Noise | 1.24 µV/sqrt(Hz) |
| **6** | Power Consumption | 18.74 µw |
| **7** | Supply voltage | ± 0.8 V |

## 9. Conclusion

The neural signal acquisition amplifier with 18.24µw and 1.24µVrms over the 100Hz – 5 KHz has been presented. A new signal processing circuit has been developed using 2 transistor reduces overall power consumption. Simulation results shows that this circuit is designed to meet all requirements for the detection and forewarning to the epilepsy affected patients for safety and clinical contexts.

## 10. Acknowledgement

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