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Wind Energy Using in Generation of proficient Power with Five-Level Dual-Buck Full Bridge Inverters

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***Abstract*: Among varied styles of renewable generation, electrical phenomenon generation, alternative energy, and fuel cells are wide used. The power density of dual-buck converters has to be improved, also because the conversion potency. In this work the simulation results of wind energy conversion system with three phase five-level DBFBI topologies are obtained through Power sim for grid application. High-efficiency converters area unit fascinating for renewable energy systems, specifically those connected with grid connected wind applications. The aim is to possess a straightforward, robust, free maintenance, and highly efficient system. The proposed five-level DBFBI topologies have been applied in a three phase wind energy system and presents several promising advantages. First, it will generate power for ac utility from PMSG. Secondly, it will increase or decreases output-voltage level with the assistance of buck-boost device to take care of constant output in order that it's higher potency and lower weight for the general system. Third, in the case of a five-level DBFBI topologies, it does not require an output filter because high-order harmonics are effectively filtered off, owing to the reactance of the inductive load; so, it will turn out a stairway voltage wave shape with lower harmonics eliminated specified higher order harmonics will be simply filtered off if required for that specific application.**

***Keywords*: Wind energy, Dual-buck inverter, efficiency, grid-tied inverter, multilevel inverter, Power density**

1. Introduction

Power MOSFETs have some attractive advantages, such as fast switching, low switching loss, and resistive conduction voltage drop. The switching frequency of the power converters using MOSFETs can be higher than that of the power converters using insulated-gate bipolar transistors (IGBTs), which benefits for reducing current ripples and the size of passive components. However, since the reverse recovery characteristic of the body diodes is poor, power MOSFETs cannot be used in conventional H-bridge inverters. In order to utilize the advantages of MOSFETs, soft-switching techniques are adopted conventionally. However, additional auxiliary switches, passive components, and more gate driving circuits are required in the soft-switching inverter, which lowers the reliability and increases the cost and complexity. In dual-buck inverters, no reverse recovery problem occurs in the freewheeling mode, since the independent freewheeling diode has excellent reverse recovery characteristic. In addition, power MOSFETs are used in dual-buck inverters. Therefore, the dual-buck inverter is an attractive solution to achieve high efficiency for low-power grid-connected applications. Two filter inductors are required in single-phase dual-buck inverters, and both of the inductors are operating at each half cycle of the utility grid alternately, which increases the size and weight of the converter. Hence, the power density of conventional two-level and three-level dual-buck inverters needs to be improved. The multilevel system is an effective way to attain high power density.

However, the number of power switches used in the multilevel inverter is more than that used in the conventional half-bridge and full-bridge inverters. Moreover, its control circuit is much more complicated. Thus, the tradeoff between the performance and the hardware cost should be considered in the design of multilevel inverters A five-level H-bridge inverter topology was proposed by introduce a neutral point clamped bi-directional switch (NPC branch) based on the conventional full-bridge inverter .Compared with the Dual Noval Power Converter five-level inverter topology, the FCC five-level inverter topology, and the ANPC five-level inverter topology, the number of power devices in the new five-level H-bridge inverter has been reduced significantly . The low-voltage (less than 1000 V) application, this five-level H-bridge inverter topology is an enhanced option than conventional multilevel inverter topologies. It is regarded as one of the best solutions for grid-tied inverters as well. In the issue of neutral point (NP) potential balancing was discussed as well, and the NP potential self-balancing of two capacitors was considered to be automatically realized. However, the NP impending self-balancing of five-level full-bridge inverters is associated to the modulation index. It provide momentous advantages over the two-level converter, but not limited to lower harmonic distortion, lower electro-magnetic interference, low stress of the semiconductor switching devices and high effectiveness In a control strategy (PID) for a Buck-Boost converter and five-

level DBFBI topologies integrating PMSG to a grid was proposed .

2. Existing system

A five-level H-bridge electrical converter topology was planned by introducing a neutral purpose clamped bi-directional switch (NPC branch) supported the traditional full-bridge electrical converter. Compared with the DNPC five-level electrical converter topology, the independent agency five-level electrical converter topology, and therefore the ANPC five-level electrical converter topology, the amount of power devices within the new five-level H-bridge electrical converter has been reduced significantly. Therefore, for the low-tension (less than a thousand V) applications, this five-level H-bridge electrical converter topology maybe higher choice than typical construction electrical converter topologies. It is thought to be one in all the most effective solutions for grid-tied inverters.

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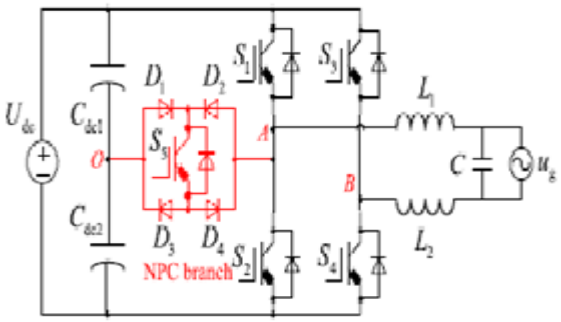

Fig. 1. Circuit diagram of existing system

3. Proposed system

In this paper, a control strategy of five-level DBFBI topologies for wind energy applications to exchange active and reactive power to grid is discussed. The required range of output voltage levels is achieved by regulation the voltage reference level that is of nice importance for reduced value and might be used for real time. The model of the turbine only supported the wind speed and also the pitch angle. The circuit topology and control methodology of the wind generation generating system is investigated with a PMSG and a consecutive ac-dc-ac power device wind conditions are favorable the wind systems can provide electricity at lowest cost. The available wind does not always produce the required amount of power as the load demands. So there must be a power electronic converter to match the power requirement of the load. Such converters are generally known as frequency converter. A frequency converter generally has two parts, a machine side converter and a grid side converter. Fig 2 shows the output of wind energy. Conventional systems are either with a two level back to back converter or a three level inverter. Using five-level DBFBI topologies it is possible to utilize the dc voltage maximum and to produce required amount of ac voltage without any large transformers.

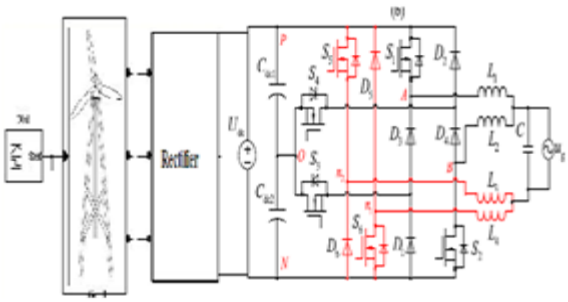

Fig. 2. Windmill of Series-diode five-level DBFBI

By employing the topology generation rule #1, a three-level DBFBI topology is combined with a two-level capacitive voltage divider and an NPC branch, as shown The nodes of the capacitive voltage divider, P1 , N1 , and O1 , are connected to the nodes P2 , N2 , and O2 , respectively. The node of the NPC branch A1 is connected to the node of the three-level DBFBI A2 .The node of the NPC branch B1 is connected to the node of the three-level DBFBI B2. Then, the redundant capacitors, Cdc1 and Cdc2, can be removed. As a result, an NPC five-level DBFBI topology is generated .On the other hand, a three-level DBFBI can be combined with a two-level half-bridge inverter by employing the topology generation rule #2, The nodes of the three level DBHBI, P1 , N1 , and O1 , are connected to the nodes P2 , N2 , and O2 , respectively.

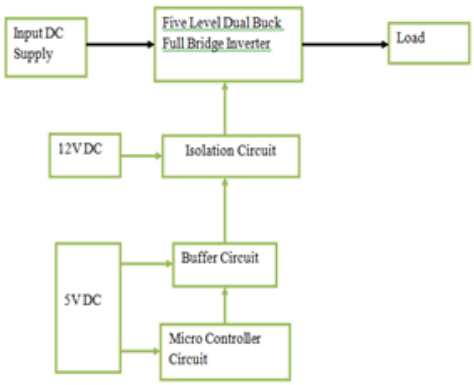

Fig. 3. Block diagram of proposed system

The node of the three-level DBHBI O1 is disconnected from the node of the utility grid n1. The node of the two-level half-bridge inverter O2 is disconnected.

4. Simulation result

The NPC five- level DBFBI topology with high reliability,

as shown in Fig. 4, is derived from an NPC three-level DBHBI combined with a two-level dual-buck half-bridge inverter. The series-switch five-level DBFBI topology with high reliability, is derived from a series-switch three level DBHBI combined with a two-level dual-buck half-bridge inverter. Similarly, the series-diode five-level DBFBI. Therefore, a family of five-level DBFBI topologies with high reliability can be generated by employing the extended topology generation rule. Although the proposed high-reliability five level DBFBI topologies are different from the topologies proposed the modulation methods and the operation modes are similar.

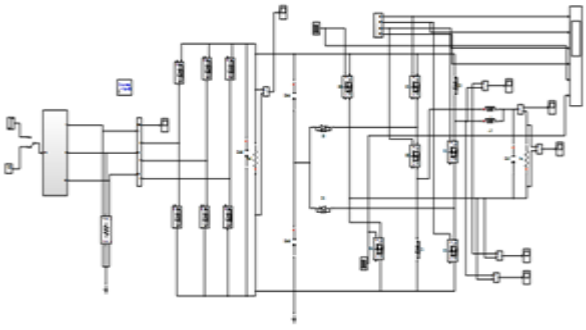

Fig. 4. Simulation circuit diagram

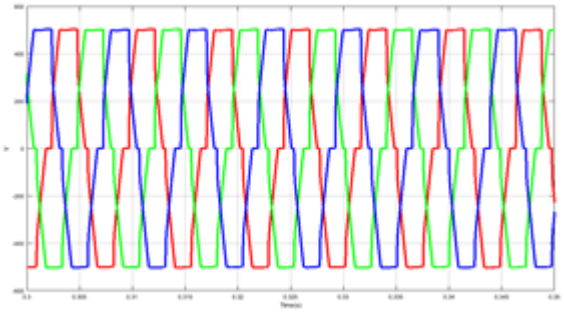

Fig. 5. Input voltage from wind

The total inductance of split inductors ($L1$ and $L4$) in high reliability five-level DBFBI topologies is the same as that of the inductor $L1$ in five-level DBFBI topology. Assume that the voltage of the utility grid is 230 V, and the frequency of the utility grid is 50 Hz. The grid-tied power in 1 kW, and the switching frequency is 40 kHz. The NP potential balancing can be realized when $M > 0.56$. The simulation results are shown in Fig. 5. It can be seen that when the modulation index is higher than 0.56, the divided input capacitor voltages are kept at self-balance However, since there two additional diodes, the hardware cost of the high reliability topologies is higher. Therefore, the following analyses on switching states, NP potential balancing and power devices losses are conducted based on the five-level DBFBI topologies Maximum negative output, uBn = $-U$dc. There is no current flowing through the inductor $L1$; thus, the voltage on the inductor $L1$ is equal to zero, and uAn = $ug < 0$. As a result, uAB−n = $-U$dc. $S2$, $S4$, and $S5$ are turned ON, and the other switches are turned OFF. The active current path at this mode is shown in Fig. 5.The reverse blocking voltage on $D4$ is equal to 0.5Udc, and the reverse blocking voltage on $D2$ is equal to Udc. During this state, the drain–source voltage on $S6$ is equal to Udc. In this mode, the inductor current $iL2$decrease linearly.

ds1 =(2ug /Udc) -1, ug>0.5Udc
ds2 =(-2ug/Udc)-1, -ug>0.5Udc
ds3 =2ug/Udc, 0<ug<0.5Udc
ds4 =-2ug / Udc, -0.5Udc<ug< 0

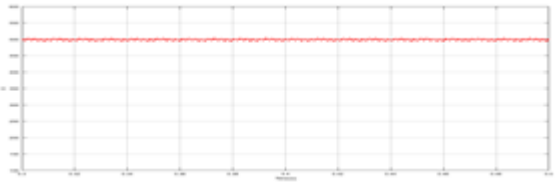

Fig. 6. Rectified DC voltage

From the above operation analysis, there is no current flowing through the body diodes of the switches. Therefore, compared with the conventional five-level H-bridge inverter topology shown in Fig. 6. rectifier dc voltage, has 500v and time 0.4s the presented five-level DBFBI topologies are free of reverse recovery problem in the freewheeling mode, and the MOSFETs with low on-resistances can be used instead of IGBTs. In addition, compared with the three-level DBFBI topology, the voltage jump of each high-frequency switch in the presented five-level DBFBI topology is only half of the input voltage. Therefore, the switching loss of the presented five-level DBFBI topology is much lower than that of the three-level DBFBI topology. Furthermore, the voltage jump of each inductor in the presented five-level DBFBI topology is only half of the input voltage as well, which means this topology features smaller filter inductance.

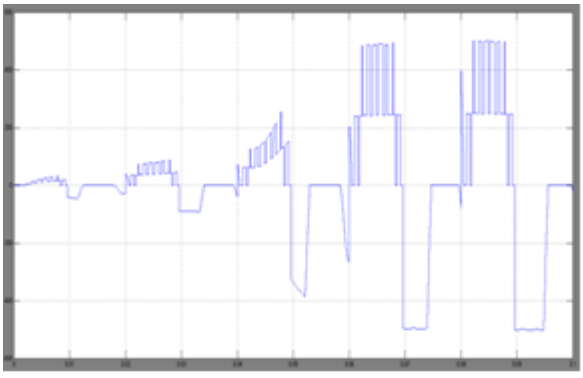

Fig. 7. Simulation results of L1 voltage

The Fig. 7 shows the waveforms of voltage in inductor Since the SiC diodes are used in DBFBI topologies, the power losses caused by the reverse recovery can be ignored. According to the data sheets of power devices, the turn-on behavior is

characterized by the device loss distributions of these four topologies under different switching frequencies are shown in. It can be seen that the thermal stress distributions of power switches in these three five-level DBFBI topologies are almost the same. From sic diodes are used in the five –level of DBFBI topologies with filter inductance of the L1 and L2 voltage formed in the both positive and negative pulse shown in Fig. 9. As the five level wave form. In addition, compared with the three-level DBFBI topology, the voltage jump of each high-frequency switch in the presented five-level DBFBI topology is only half of the input voltage.

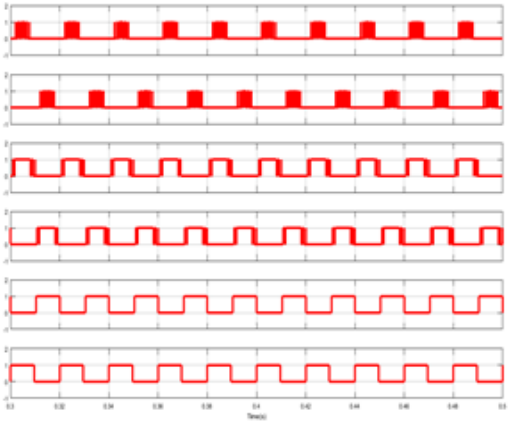

Fig. 8. Gate pulses

From the Fig. 8, pulse width modulation (PWM) of the gate pulse is a square waveform and time 0.4 sec is used the gate pulse.

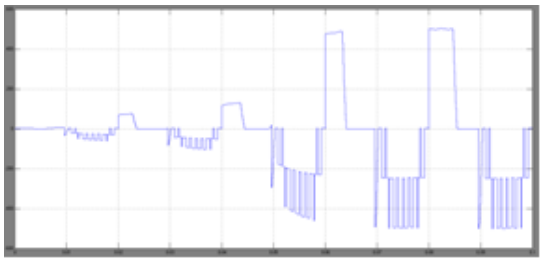

Fig. 9. Simulation results L2 Voltage

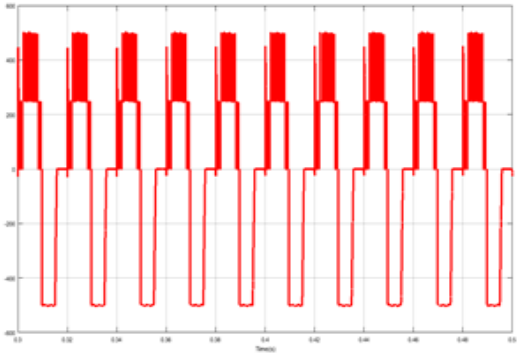

Fig. 10. Simulation result of Vo1

Furthermore, the voltage jump of each inductor in the presented five-level DBFBI topology is only half of the input voltage as well, which means this topology features smaller filter inductance. Fig. 10, as well as shown in voltage level increased with the range of 450v and time 0.4sec of the voltage wave forms positive side of DBFBI topologies.

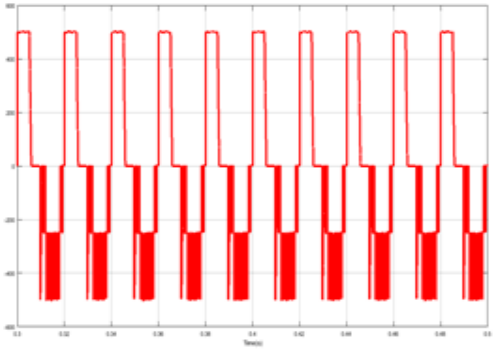

Fig. 11. Simulation result of Vo2

From the five level DBFBI topologies are formed as shown Fig. 11 voltages level two has to increase with the negative pulse waveform occurred at 400voltages to 450 voltages . The input voltage, and the voltage jump of two switches is equal to half of the input voltage, it can be seen that the maximum drain–source voltage.

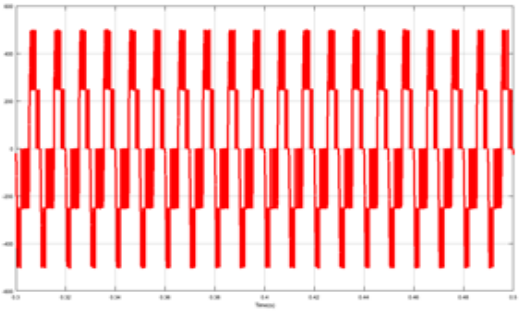

Fig. 12. Simulation result of V03

The experimental results of the series-switch five-level DBFBI are shown in Fig. 12, where *ug* and *ig* represent the grid voltage and the grid-tied current, respectively. *u*An and *u*Bn represent the voltages *A* to *n* and *B* to *n*, respectively. *uL*1and *uL*2 represent the voltages of filter inductors *L*1 and *L*2 respectively.*u*S1, *u*S2, and *u*S3 represent the drain–source voltage on the switch *S*1, the switch *S*2, and the switch *S*3 , respectively.*u*D2 represents the reverse blocking voltage on *D*2 .From Fig. 12, it can be seen that the series-switch five-level DBFBI operates with uniploar modulation, and the series-switch five-level DBFBI has five output voltage levels.

Furthermore, since the *u*AB−n waveforms of the three five-level DBFBI topologies Fig. 14, shown in the same, the filter inductor losses of the three five-level DBFBI topologies, with the same output power, the same inductor current ripple and the same switching frequency, are the same. Therefore, the inductor power losses of the three five-level DBFBI topologies are not calculated. However, compared with the three-level DBFBI topology, both the value and the volume of filter inductors in

the five-level DBFBI topologies are smaller. Therefore, the inductor loss of proposed five-level DBFBI topologies is smaller than that of the three-level DBFBI topology .The experimental results of the series-diode five-level DBFBI, where *u*S1, *u*S2, and *u*S3 represent the drain–source voltage on the switch *S*1, *S*2 , and *S*3 , respectively. *u*D3 represents the reverse blocking voltage on *D*3 . it can be seen that both of the maximum drain–source voltages on *S*1 and *S*2 are equal to the input voltage, and the voltage jump of two switches is equal to half of the input voltage.), it can be seen that the maximum drain–source voltage on *S*3 is equal to half of the input voltage, while the maximum drain–source voltage on *D*3 is equal to the input voltage. This result verifies the analysis of voltage stresses.

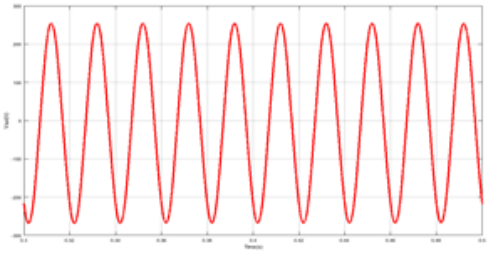

Fig. 13. Simulation result of output voltage

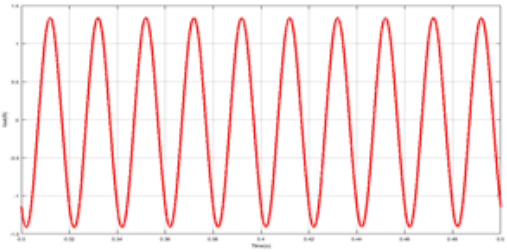

Fig. 14. Simulation result of output current

5. Conclusion

This paper deals with the exploration, modeling and control system for permanent magnet synchronous generator (PMSG) based wind turbine connected to the grid. A wind energy conversion using DC-DC Buck- Boost Converter for permanent magnet synchronous generator (PMSG) based variable speed wind energy conversion system (WECS) has been proposed which is integrated with grid using five-level DBFBI topologies. In order to enhance the reliability of five-level DBFBI topologies, an extended five-level DBFBI topology generation method has been proposed. The two-level half-bridge inverter is replaced by a two-level dual-buck half-bridge inverter, and a family of five level DBFBI topologies with high reliability has been generated. Furthermore, the relationship between the NP potential self-balancing and the modulation index of inverters is revealed. Experimental results have verified that the five-level DBFBI topologies have the following Advantages:

1. Compared with the three-level DBFBI, the voltage jumps of high-frequency switching devices and the filter inductances are only half. Therefore, the family of five-level DBFBI topologies requires lower power rating devices and smaller filter inductors, which result in higher conversion efficiency and higher power density.
2. The series-switch five-level DBFBI has the highest CEC efficiency compared with the three-level DBFBI, the conventional five- level H-bridge inverter, the NPC five-level DBFBI, and the series-diode five-level DBFBI.

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