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Input-Based Dynamic Reconfiguration of Approximate Arithmetic Units for Video Encoding

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***Abstract*: The field of approximate computing has received significant attention from the research community in the past few years, especially in the context of various signal processing applications. Image and video compression algorithms, such as JPEG, MPEG, and so on, are particularly attractive candidates for approximate computing, since they are tolerant of computing imprecision due to human imperceptibility, which can be exploited to realize highly power-efficient implementations of these algorithms. However, existing approximate architectures typically fix the level of hardware approximation statically and are not adaptive to input data. For example, if a fixed approximate hardware configuration is used for an MPEG encoder (i.e., a fixed level of approximation), the output quality varies greatly for different input videos. This paper addresses this issue by proposing a reconfigurable approximate architecture for MPEG encoders that optimizes power consumption with the goal of maintaining a particular Peak Signal-to-Noise Ratio (PSNR) threshold for any video. Toward this end, we design reconfigurable adder/subtractor blocks (RABs), which have the ability to modulate their degree of approximation, and subsequently integrate these blocks in the motion estimation and discrete cosine transform modules of the MPEG encoder. We propose two heuristics for automatically tuning the approximation degree of the RABs in these two modules during runtime based on the Characteristics of each individual video.**

***Keywords*: Signal-to-Noise Ratio, assessment technique and MPEG encode**

1. Introduction

The merit of the encoding operation can be determined from the output quality of the decoded video. Objective metrics, such as Peak Signal-to-Noise Ratio (PSNR), and so on have a very good correlation with the subjective procedures of measuring the quality of the videos. Hence, we have utilized the popular and simple PSNR metric as a means of video quality estimation. PSNR is a full-reference video quality assessment technique, which utilizes a pixel-to-pixel difference with respect to the original video. PSNR of a video is defined as the average PSNR over a constant number of frames (50) of the video. Images and videos differ in a variety of properties, such as color, resolution, brightness, contrast, saturation, blur, format, and so on.

Thus, a naive static approximation technique, which provides satisfactory viewing quality for some specific types of videos, will fail to give adequate quality for some others. In that case, the viewing experience is significantly worsened if the approximate mode is not customized for the present type of video being watched. This is not possible for fixed hardware, and therefore a need arises for reconfiguring the architecture based on the characteristics of the video being viewed. To support this claim, present the PSNR variation of different videos when encoded using an MPEG encoder that used a fixed approximation technique. An approximation mode, we have chosen approximation mode 5 from for implementing the fixed approximation hardware. We replaced all the adders/ subtractors in the ME and the DCT blocks with approximate versions. There has been a considerable measure of effort in constructing energy efficient video pressure plans. A large number of them are identified with the specific instance of a MPEG encoder. Diverse strategies for control lessening incorporate algorithmic modifications voltage over-scaling, and loose calculation of measurements. The presentation of surmised registering strategies has opened up completely new open doors in building low-control video pressure designs. Inexact figuring strategies accomplish a lot of energy reserve funds by presenting a little measure of blunder or mistake into the rationale square. Distinctive methodologies for estimate incorporate blunder presentation through voltage overscaling, clever rationale control, and circuit simplification utilizing couldn't care less based improvement procedures. The techniques present imprecision by supplanting adders with their surmised partners. The rough adders are gotten by cleverly erasing a portion of the transistors in a mirror viper. An imperative point to note is that these estimated circuits are hardwired and can't be modified without resynthesizing the whole circuit. There additionally exist occasions of approximations presented in a MPEG encoder. The majority of them misuse the inalienable mistake strength of the movement estimation (ME) calculation, which brings about minor quality debasement.

For instance, utilize a bit width pressure method to decrease control utilization of video outline memory. Utilize bit truncation to present approximations in the ME square of a

MPEG encoder. A versatile piece covering strategy is proposed in, where the creators propose to truncate the pixels of the present and past edges required for ME relying on the quantization step. Be that as it may, such a coarse-grained input truncation is relevant just to the specific instance of ME and gives unsuitable outcomes for different pieces, for example, discrete cosine change (DCT), which requires a finer direction over blunder. As in, this paper likewise points in approximating the adders of the ME and DCT squares of a MPEG encoder. Be that as it may, this paper presents the idea of reconfigurable guess, which, as we will show, helps in maintaining better control over application-level quality measurements while at the same time procuring the power utilization benefits of equipment estimate. This paper incorporates some of extra elements as depicted here. We expand the heuristics for regulating the DA of the reconfigurable equipment hinders by including the component of most significant bit (MSB) truncation, which enhances the vitality quality tradeoff amid the video encoding process. We likewise stretch out the RAB to incorporate three extra viper models, viz., CLA, CBA, and CSA. Also, for the convey look ahead based RAB, we propose double mode convey look ahead and spread produce obstructs as its constituent essential building pieces. At long last, we give a near investigation of the power utilization of the distinctive RABs and furthermore exhibit how the DA is naturally directed crosswise over various edges amid run-time.

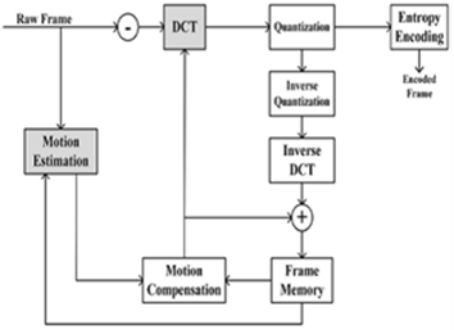

Fig. 1. MPEG encoder block diagram

2. Proposed System Main Modules

- 1-bit DMFA
- 8-bit reconfigurable RCA block.
- 1-bit dual-mode carry propagate generate blocks. 8-bit reconfigurable CLA block.

A. Bit DMFA

Dynamic variation of the DA can be done when each of the adder/subtractor blocks is equipped with one or more The latter one can also be conceptualized as an enhanced version of truncation as it just relays the two 1-bit inputs, one as Sum and the other as Carry Out In case A, B, and C_{in} are the 1-bit inputs to the full adder (FA), then the outputs are Sum = B and C_{out}= A. The proposed scheme replaces each FA cell of the adders/subtractors with a dual-mode FA (DMFA) cell in which each FA cell can operate either in fully accurate or in some approximation mode depending on the state of the control signal APP. It is important to note that the FA cell is power-gated when operating in the approximate mode. Our experiments have shown a negligible difference in the power consumption of DMFA when operated in either of the two approximation modes. Hence, without any loss of generality, approximation 5 was chosen for its higher probability of giving the correct output result than truncation, which invariably outputs 0 irrespective of the input. The logic block diagram of the DMFA cell, which replaces the constituent FA cells of an 8-bit RCA In addition, it also consists of the approximation controller for generating the appropriate select signals for the multiplexers. A multimode FA cell would provide even a better alternative to the DMFA from the point of controlling the approximation magnitude. However, it also increases the complexity of the decoder block used for asserting the right select signals to the multiplexers as well as the logic overhead for the multiplexers themselves. This undermines the primary objective as most of the power savings that we get from approximating the bits are lost. Instead, the two-mode decoder and the 2:1 multiplexers have negligible overhead and also provide sufficient command over the approximation degree.

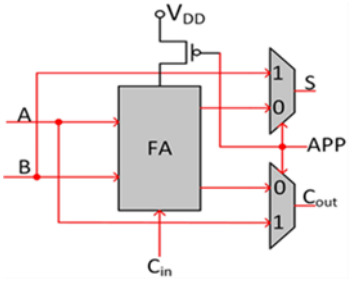

Fig. 2. 1-bit DMFA

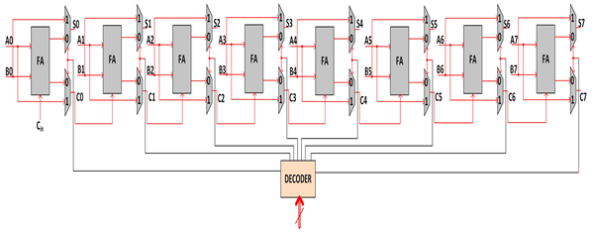

Fig. 3. 8-bit reconfigurable RCA block

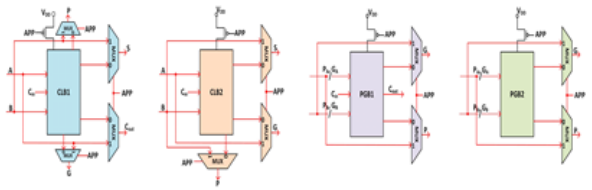

Fig. 4. 1-bit dual-mode carry propagate generate blocks.

B. 8-Bit Reconfigurable RCA block

Other varieties, like CLA and tree adders, use different types of carry propagate and generate blocks as their basic building units, and hence require some additional modifications to

function as RABs. As an example, we implemented a 16-bit CLA consisting of four different types of basic blocks depending upon the presence of sum (S), C_{out}, carry propagation (P), and carry generation (G) at different levels. We address the basic blocks present at the first (or lowermost) level of a CLA, which have inputs coming in directly, as carry look ahead blocks, CLB1 and CLB2.

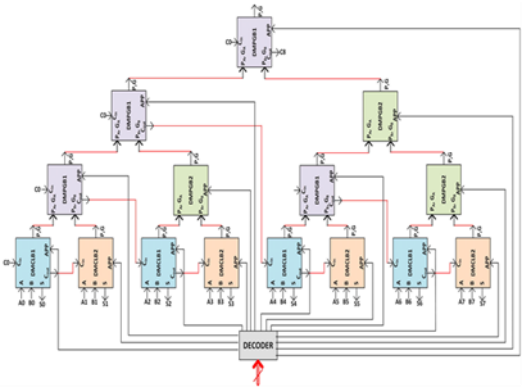

Fig. 5. 8-bit reconfigurable CLA block

The difference among them being that CLB1 produces an additional C_{out} signal compared with CLB2. Their corresponding dual-mode versions, DMCLB1 and DMCLB2, have both S and P approximated by input operand B and both C_{out} and G approximated by input operand A, as shown in Fig. The basic blocks present at the higher levels of CLA hierarchy are denoted as propagate and generate blocks, PGB1 and PGB2. In this case, PGB1 produces an extra C_{out} output as compared with PGB2. As shown in the configurable dual-mode versions, DMPGB1 and DMPGB2, use inputs PA and GB as approximations for outputs P and G, respectively, when operating in the approximate mode. These approximations were selected empirically ensuring that the ratio of the probability of correct output to the additional circuit overhead for each of the blocks is large For a reconfigurable CLA, DMCLB1 and DMCLB2 blocks are approximated in accordance with the DA. However, the DMPGB1 and DMPGB2 blocks are approximated only when each and every DMCLB1, DMCLB2, DMPGB1, and DMPGB2 block, which belongs to the transitive fan-in cones of the concerned block, is approximated. Otherwise, the block is operated in the accurate mode. For example, any DMPGB block at the second level of CLA can be made to operate in approximate mode, if and only if, both of its constituent DMCLB1 and DMCLB2 blocks are operating in the approximate mode. Similar protocol is ensued for the blocks residing at higher levels of the tree, where each DMPGB block can be approximated only when both of its constituent DMPGB1 and DMPGB2 blocks are approximated. This architecture can be easily extrapolated to other similar type CLAs. Similar protocol is ensued for the blocks residing at higher levels of the tree, where each DMPGB block can be approximated only when both of its constituent DMPGB1 and DMPGB2 blocks are approximated. This architecture can be easily extrapolated to other similar type CLAs.

3. Simulation results

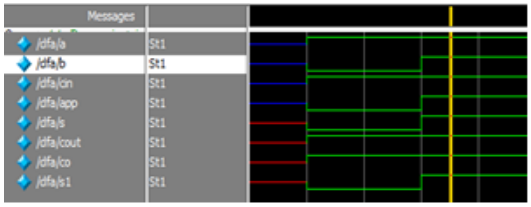

Fig. 6. 1-bit DMFA

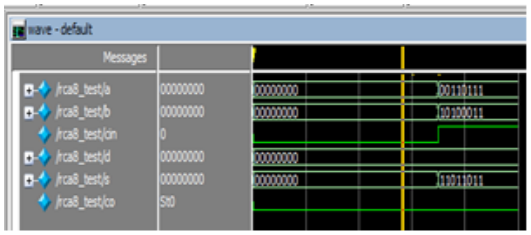

Fig. 7. 8-bit reconfigurable RCA block

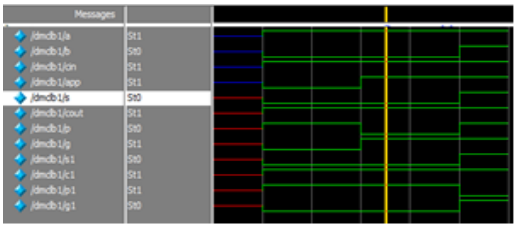

Fig. 8. 1-bit dual-mode carry propagate generate blocks

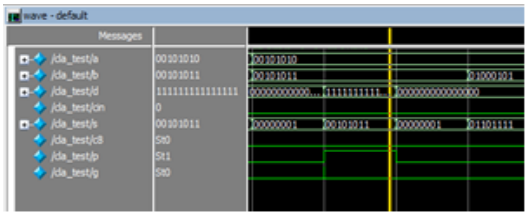

Fig. 9. 8-bit reconfigurable CLA block

4. Conclusion

We proposed a reconfigurable approximate architecture for the MPEG encoders that optimize power consumption while maintaining output quality across different input videos. The proposed architecture is based on the concept of dynamically reconfiguring the level of approximation in the hardware based on the input characteristics. It requires the user to specify only the overall minimum quality for videos instead of having to decide the level of hardware approximation. Our experimental results show that the proposed architecture results in power savings equivalent to a baseline approach that uses fixed approximate hardware while respecting quality constraints across different videos. Future work includes the incorporation of other approximation techniques and extending the approximations to other arithmetic and functional blocks.

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