International Journal of Research in Engineering, Science and Management
Volume-1, Issue-11, November-2018
www.ijresm.com | ISSN (Online): 2581-5792

Design of High Speed and Power Efficient Full Subtractor Using MTCMOS

Shaik Nazia Tarannum[1], M. Raju[2], B. Ram Prasad[3]
[1]*M. Tech. Student, Department of ECE, WITS, Warangal, India*
[2,3]*Assistant Professor, Department of ECE, WITS, Warangal, India*

***Abstract*: In this paper a full subtractor is designed using MTCMOS technique. Combinational logic circuit has extensive applications in quantum computing and low power VLSI design. The rapid increase in the number of transistors on chips has enabled a dramatic increase in the performance of computing systems. To achieve higher density and performance and lower power consumption MTCMOS devices have been scaled for more than 30 years. The MTCMOS is a Multi Threshold Complementary Metal Oxide Semiconductor technique is proposed to reduce the leakage current and leakage power also and got better result as compared to standard half subtractor cell. Low-power design techniques proposed to minimize the active leakage power in nano scale CMOS very large scale integration (VLSI) systems. Using MTCMOS approach compare leakage current and leakage power of full subtractor in active mode. Leakage current in proposed full subtractor is reduced compared to conventional full subtractor. Simulation result is performed at 0.7 volt using cadence virtuoso tool in 45nanometer technology. Finally, the paper explores different circuit techniques to reduce the leakage power consumption.**

***Keywords*: Power Dissipation, VLSI, Leakage, MTCMOS, Tanner.**

1. Introduction

The increase of transistors on chips has enabled a dramatic increase in the performance of computing systems. The performance improvement has been accompanied by an increase in power dissipation. That's why requiring more expensive packaging and cooling technology. The Power dissipation in CMOS circuits has been the charging and discharging of load capacitances, often referred to as the dynamic power dissipation. MOSFETs are fabricated with high overall doping concentration, lowered source/drain junction depths, halo doping, high-mobility channel materials, etc. Furthermore, the reduction of the gate oxide thickness causes a drastic increase in the gate tunneling leakage current due to carriers tunneling through the gate oxide, which is strong exponential function of the voltage magnitude across the gate oxide. Consequently, to minimize the leakage power in active mode. The rapid increase in the number of transistors on chips has enabled a dramatic increase in the performance of computing systems. IN MODERN digital integrated circuits, power consumption can be attributed to three main components.

2. Project back ground

A. *Power gating*

Power gating affects design architecture more than clock gating. It increases time delays as power gated modes have to be safely entered and exited. Architectural trade-offs exist between designing for the amount of leakage power saving in low power modes and the energy dissipation to enter and exit the low power modes. Shutting down the blocks can be accomplished either by software or hardware. Driver software can schedule the power down operations. Hardware timers can be utilized [1]. A dedicated power management controller is another option. An externally switched power supply is a very basic form of power gating to achieve long term leakage power reduction. To shut off the block for small intervals of time, internal power gating is more suitable. CMOS switches [2] that provide power to the circuitry are controlled by power gating controllers. Outputs of the power gated block discharge slowly. Hence output voltage levels spend more time in threshold voltage level. This can lead to larger short circuit current. Power gating uses low-leakage PMOS transistors as header switches to shut off power supplies to parts of a design in standby or sleep mode [4].

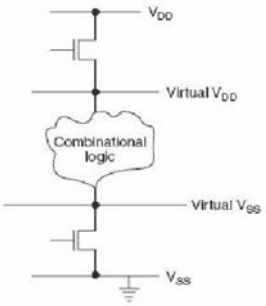

Fig .1. Power gated circuits

NMOS footer switches can also be used as sleep transistors. Inserting the sleep transistors splits the chip's power network into a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off.

B. *Power-gating parameters*

Power gating implementation has additional considerations

for timing closure implementation. The following parameters need to be considered and their values carefully chosen for a successful implementation of this methodology.

1) Power gate size

The power gate size must be selected to handle the amount of switching current at any given time. The gate must be bigger such that there is no measurable voltage (IR) drop due to the gate. As a rule of thumb, the gate size is selected to be around 3 times the switching capacitance. Designers can also choose between header (P- MOS) or footer (N-MOS) gate. Usually footer gates tend to be smaller in area for the same switching current. Dynamic power analysis tools can accurately measure the switching current and also predict the size for the power gate.

2) Gate control slew rate

In power gating, this is an important parameter that determines the power gating efficiency. When the slew rate is large, it takes more time to switch off and switch-on the circuit and hence can affect the power gating efficiency. Slew rate is controlled through buffering the gate control signal.

3) Simultaneous switching capacitance

This important constraint refers to the amount of circuit that can be switched simultaneously without affecting the power network integrity. If a large amount of the circuit is switched simultaneously, the resulting "rush current" can compromise the power network integrity. The circuit needs to be switched in stages in order to prevent this.

4) Power gate leakage

Since power gates are made of active transistors, leakage reduction is an important consideration to maximize power savings.

C. Leakage Reduction Techniques

1) M T C M O S

The low-power and high performance design requirements of modern VLSI technology can be achieved by using MTCMOS technology. Low, normal and high threshold voltage transistors are used to design a CMOS circuit in this technique. With the scaling of CMOS technology, Supply and threshold voltages are reduced. Sub threshold leakage current increases exponentially with lowering of threshold voltage.

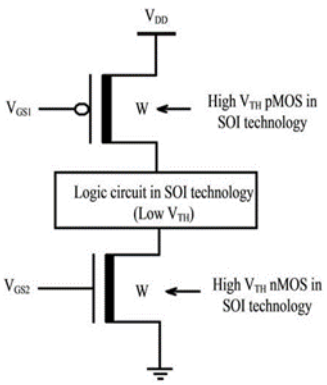

Fig .2. General MTCMOS circuit architecture

Multi-threshold CMOS (MTCMOS) is a design technique in which high threshold sleep transistors are connected between the logic circuit and power or ground, thus creating a virtual supply rail or virtual ground rail, respectively. The low-threshold voltage transistors which have high performance are used to reduce the propagation delay time in the critical path. The high-threshold voltage transistors which have less power consumption are used to reduce the power consumption in the shortest path [4], [5]. Fig. 2 shows MTCMOS circuit technology which satisfies both the requirements of lowering the threshold voltage to obtain high speed and reducing standby current to have low power.

D. Full Subtractor

A full subtractor is a combinational circuit that performs a subtraction between two bits taking into account that a 1 may have been borrowed by a lower significant stage. This circuit has three inputs and two outputs.

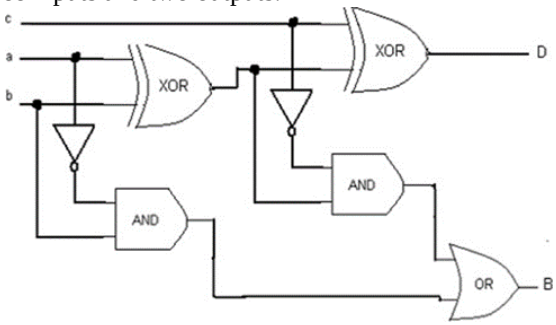

Fig .3. Gate Level Full Subtractor Circuit

A logic Circuit which is used for Subtracting three single bit binary numbers is known as Full Subtractor. The Truth table of Full Subtractor is shown below of Table 1.

Table 1
Truth Table of Full Subtractor

Full Subtractor-Truth Table				
Input			Output	
A	B	C	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

1) Variable body bias

This is another new leakage reduction technique, which we call the „"Variable body Biasing. The body effect in CMOS transistors, of the depletion layer leads to lower biasing of CMOS transistor increase forward biasing of the COMS transistor and also in CMOS threshold voltage increased doping of the channel but applied bias. Therefore the current in th region can be partially decreased.

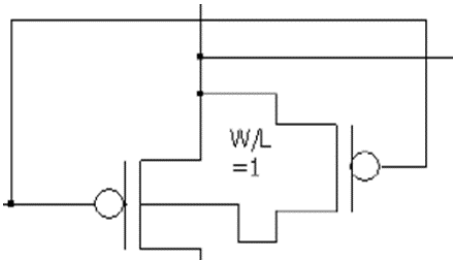

Fig. 4. Boby bias structure

3. Results

The below Fig. 5 shows that the circuit of full subtractor and Figure shows that the simulation results of Full Subtractor.

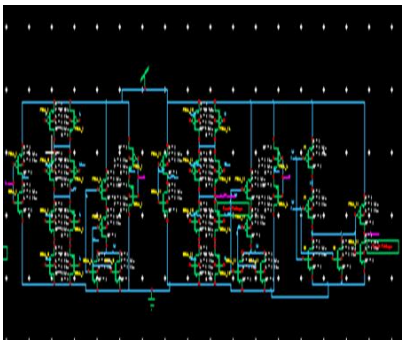
Fig. 5. Tanner design of full subtractor

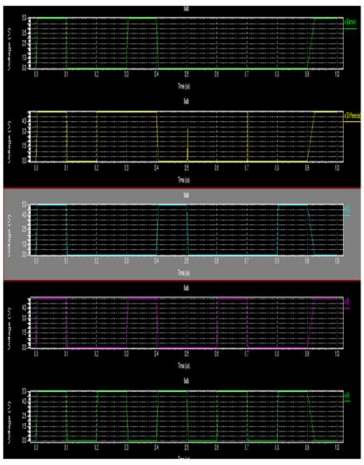
Fig. 6. Simulation of full subtractor

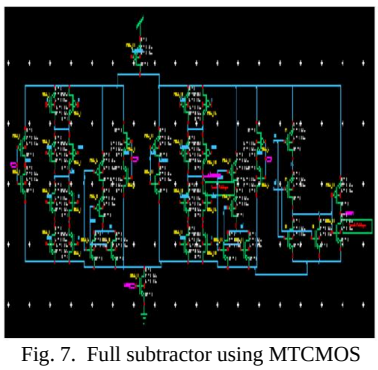
Fig. 7. Full subtractor using MTCMOS

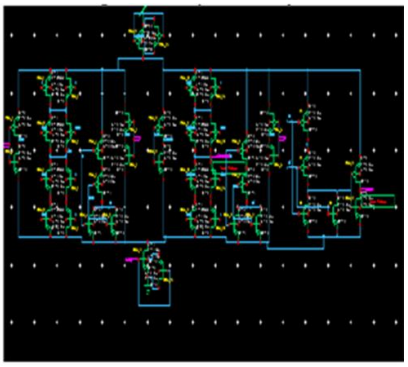
Fig .8. Full subtractor using variable body bias technique

4. Conclusion

In this Full Subtractor is designed with different leakage power reduction techniques like MTCMOS, Variable Body-Bias technique. Proposed method is an effective circuit level technique that enhances the performance and provides low design methodologies by using both low and high threshold voltage transistors. From Simulation results it is concluded that proposed method1 effectively reduces leakage power.

References

[1] Active Leakage Current Control and Minimization in CMOS VLSI Circuits" IEICE Transactions, 2005, pp. 509-519.
[2] Kaushik Roy, Saibal Mukhopadhyay and Hamid Mahmoodi-Meimand, "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Sub micrometer CMOS Circuits," proceedings of the IEEE, vol. 91, no. 2, February 2003.
[3] James T. Kao and Anantha P. Chandrakasan, "Dual- Threshold Voltage Techniques for Low-Power Digital Circuits," IEEE Journal of Solid-State Circuits, vol. 35, no. 7, JULY 2000.
[4] Shyam Akashe, Nitesh Kumar Tiwari, Jayram Shrivas and Rajeev Sharma, "A Novel High Speed & Power Efficient Half Adder Design Using MTCMOS Technique in 45 Nanometre Regime" IEEE International Conference on Advanced Communication Control and Computing Technologies (ICACCCT) 2012.
[5] Milind Gautam and Shyam Akashe, "Reduction of Leakage Current and Power in Full Subtractor Using MTCMOS Technique" 2013 International Conference on Computer Communication and Informatics (ICCCI - 2013), Jan. 04 – 06, 2013.
[6] J. Jaffari and A. Afzali-Kusha, "New Dual-Threshold Voltage Assignment Technique for Low-Power Digital Circuits," pp.413-416 IEEE 2004.
[7] L. Wei. 2. Chen, K. Roy, M. C. Johnson, Y. Ye and V. De, "Design and optimization of dual threshold circuits for low voltage low power applications," IEEE Transactions on VLSI Systems. Vol. 7. No. 1, pp. 16-24. Mar. 1999.
[8] B. Dilip1, P. Surya Prasad2 & R. S. G. Bhavani3 "Leakage Power Reduction In CMOS Circuits Using Leakage Control Transistor Technique In Nanoscale Technology" International Journal of Electronics Signals and Systems (IJESS), Vol-2 Issue-1, 2012.