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Design, Simulation and Layout of Low Drop-Out (LDO) Voltage Regulator

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***Abstract*: In this paper a low voltage, low-dropout (LDO) voltage regulator that is capable of providing regulated output with small drop-out voltage design procedure is proposed. The entire circuit has been designed using gpdk045 nm technology and simulated using cadence virtuoso tool. It discusses a 1.5V, 30mA CMOS low drop-out linear voltage regulator with a compensation capacitor of 4pF and nulling resistor of 4KΩ. The experimental result show that the maximum output load current is 30mA and the regulated output voltage is 1.5V. The regulator provides a full load transient response with less than 5mV overshoots and undershoots. The active layout area is 187.035µm x 133.52µm.**

***Keywords*: Area, Low drop-out (LDO) regulator, PSRR, Quiescent current, 45nm CMOS Technology.**

1. Introduction

The electronic industry focus its limits on management of power systems as the modern devices size are greatly decreasing and the efficiency of the battery is not increased as much. Thus leading to system on chip (SOC) where both Analog and Digitals are fabricated on the very same die. This leads to the utilization of the voltage regulator, Switching Regulator, DC-DC converter or their combinations as they will be needed for power supply for different building blocks. LDO (Low Dropout voltage regulator) are linear regulator which required less voltage difference between its input and output to properly regulate the input voltage.

LDO becomes one of the fundamental building blocks in many portables powers system as they provide stable output voltage independence of load impedance, temperature and variation of the input voltage. Thus improves the stability and noise reduction for the subsequent circuits. LDO can provide multiple voltage levels and is also has the capability of minimizing current consumption down to microamperes. Thus we can achieve low current consumption for the sub-block while in sleep mode.

Since LDO operates with a low dropout voltage and technology trends focus on designing circuit which operates on low supply voltage. They can be used for many portables electronics sub-circuits. The ability to reject or suppress supply voltage noise by shielding the noise is an important characteristic of a linear regulator.

2. Literature Survey

The [1] studies the design topologies and challenges of low power integrated low drop-out voltage regulator. [2] present the implementation of a CMOS Linear Voltage Regulator used to power up bio-implemented system. [3] proposed a LDO of low supply and low drop-out, [4] [5] papers proposed off-chip capacitors less with low quiescent current LDO, [6], [7], [8] papers deal with ultra-low quiescent current, [9] says the important issues to the emergence and design of the LDO, [10] discussed many topology of band gap reference

3. LDO Block Diagram

Fig. 1 gives the basic block diagram of a LDO regulator. As we can see it comprises of error amplifier, pass element and a feedback network. The feedback network is a resistor voltage divider which gives output voltage scaled to be approximately equal to the reference voltage applied. The two voltages i.e. reference voltage (V_{REF}) and feedback voltage (V_{FB}) is compared constantly and amplified the difference. The pass element is drive by the output of the error amplifier to keep the voltage level at the desired value.

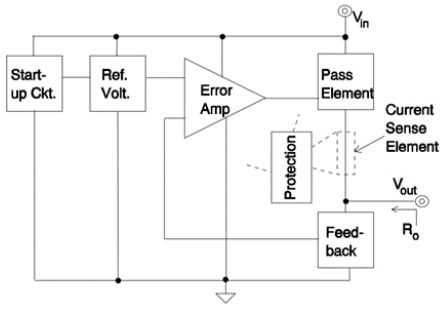

Fig. 1. Block diagram of Low Drop-Out Voltage Reference

4. Design and Implementation

A. *Band Gap Reference Voltage (BGR)*

BGR provide a voltage reference independent of the absolute

temperature. This BGR output voltage is the reference voltage V_{REF} to the error amplifier. Temperature independent can be achieved by summing up the PTAT (Proportional to absolute Temperature) and CTAT (Complementary to absolute Temperature) so that they cancelled each other temperature coefficient to give a constant voltage regardless of how the temperature changed.

CTAT is designed by giving constant current I_E to the emitter of *BJT* shorting base and collector to ground (i.e. same potential) on a PNP BJT as shown in fig. 2. PTAT also designed by taking the voltage difference of the two CTAT, so that they cancelled the CTAT nature, thus the resulting output is PTAT in nature as shown in fig. 3.

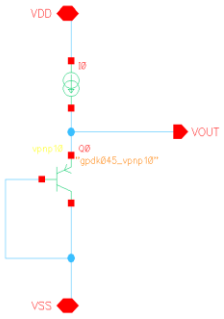

Fig. 2. CTAT Design

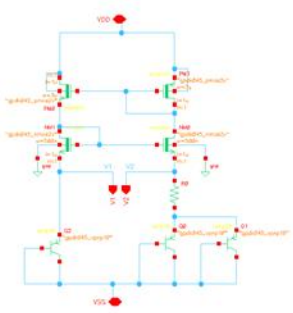

Fig. 3. PTAT Design

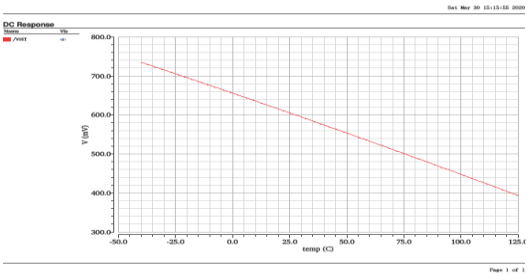

Fig. 4. Simulation of CTAT

Op-amp based BGR schematic is shown in fig. 4 the op-amp used here is for supplying constant current to the BJTs and the op-amp used 20µA current and is supplied by biasing circuit. Op-amp based BGR gives more accurate voltage when compares with current mirror based. The op-amp used has a loop gain of offset voltage of 55.16141 mV, slew rate of 8.596M, ICMR (Input Common Mode Range) of 300mV to 1.1V, CMRR (common mode rejection Ratio) 63.48 dB and PSRR (Power Supply Rejection Ratio) of 58.46 in positive and 52.44 in negative at 100 Hz respectively.

The targeted output voltage of the BGR i.e. Reference Voltage (V_{REF}) is 1.2V with the supply VDD of 1.8V. And we got the V_{REF} of 1.191675 V at 27 degree Celsius. The resistors value are R_1=2KΩ and R_2=24KΩ. The minimum value is 1.189V and maximum is 1.208V.

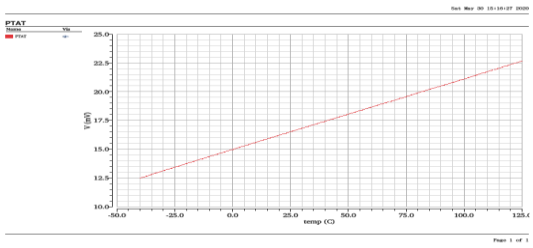

Fig. 5. Simulation of PTAT

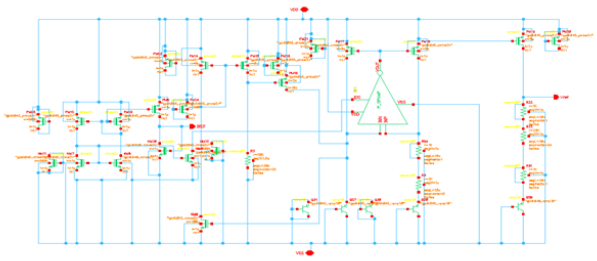

Fig. 6. Final schematic of band gap reference

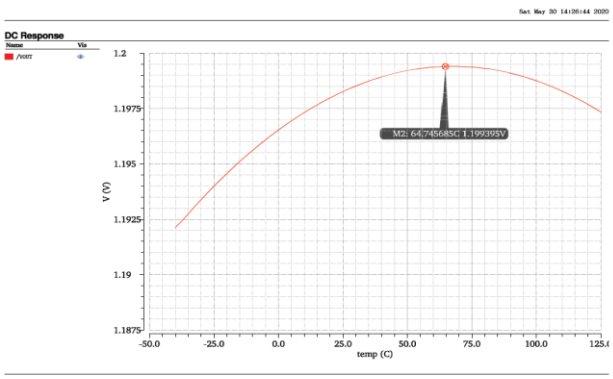

Fig. 7. Simulation result of V_{REF}

B. *Pass Element*

From the input voltage of 1.8V and output voltage of 1.5V we can derive, that maximum dropout voltage can be 300mV. I used PMOS as pass element, we can use pass transistor as NMOS but since the input voltage is low a charge pump would be needed, to raise the gate voltage of the NMOS pass transistor. This will further complicate our circuit and adding

charge pump would be inefficient in terms of power consumption. Since the maximum load current that will be flowing through the pass transistor is 30mA. In order to put the pass transistor in saturation under all load conditions of 50Ω, the aspect ratio can be calculated using the square-law equation for drain current as:

$I_D = 1/2 \mu n C_{ox} W/L (V_{GS} - V_{TH})^2$

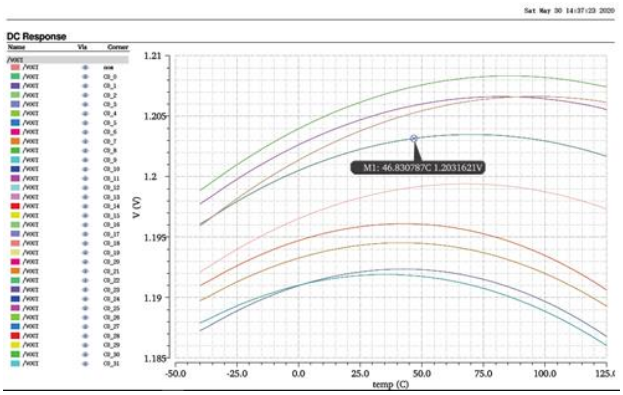

Fig. 8. Corners Analysis with 10% VDD variation from -40 to +125°C

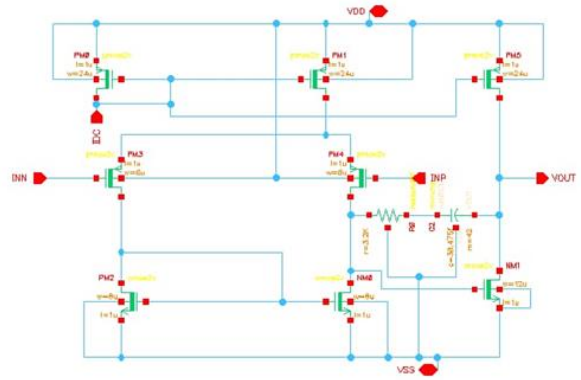

Fig. 9. Schematic of Op-amp

C. Error Amplifier (OTA)

A symmetrical OTA (operational trans-conductance amplifier) is used as error amplifier. The schematic is in fig 3.9. Compared to single OTA with differential pair, it has two more current branches, so it has larger quiescent current, but the main advantage of this topology is its large output swing. The minimum and maximum voltage at its output is limited only by the saturation voltage of the two transistors. So the minimum output voltage is the saturation voltage of the NMOS.

$$V_{OE,min} = V_{DS,sat}$$

And the maximum is the saturation voltage of PMOS at the output stage.

$$V_{OE,mix} = V_{IN} - V_{DS,sat}$$

This ensures that the error amplifier can drive the pass transistor properly over specific load current conditions.

Since the output voltage of the OTA has to drive the pass transistor, the W/L_4 and W/L_6 need to be high in order to able to drive the pass transistor of 30mA load.

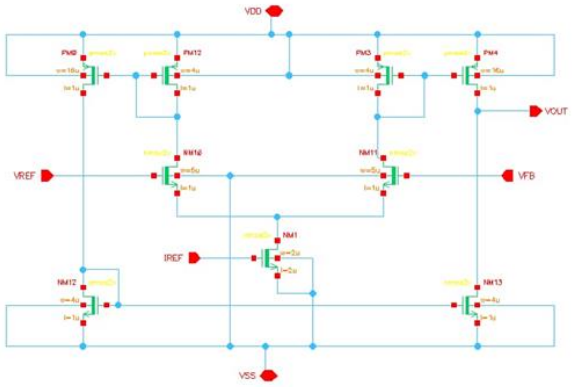

Fig. 10. Schematic of Error Amplifier (OTA)

D. Feedback Network

Resistor divider network is used as a feedback network. Since the pass transistor drain's current need to 30mA under 50Ω load condition, the total resistance value should be R_{total} = 150KΩ. Then the voltage required to the input of the OTA need to be 1.2V, the upper and lower resistors value i.e. R_3 and R_4 value can be 30K Ω and 120KΩ respectively. Since we got approximately 1.22V as Reference voltage, we put the resistors value as 32K Ω and 118K Ω instead.

The final schematic of the LDO voltage regulator is shown in fig. 11. A resistor of 2KΩ and capacitor of 1pF is used as a compensation to improve stability of the regulator.

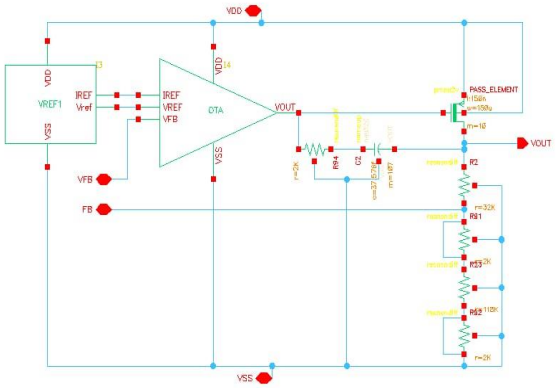

Fig. 11. Final schematic of LDO

5. LDO Simulation Results

The simulation results are shown as in followings tables and figures.

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Table 1
LDO Stability Analysis and comparison between pre and post layout simulation

	Calculation Minimum						Maximum					
	Value						Value					
	corner	cap_setup	temperature	Vdd	Pre_layout	Post_layout	corner	cap_setup	temperature	Vdd	Pre_layout	Post_layout
Gain Margin	sf	ff_min	-40	1.98	10.21	36.67	ss	ff_min	125	1.62	10.21	40.74
Gain Margin Frequency	ss	ff_min	125	1.62	28.82 M	69.07M	ff	ff_min	-40	1.98	28.82M	223.8 M
Loop Gain	ss	ff_min	125	1.62	12.11	50.06	ff	ff_min	-40	1.98	12.11	50.7
Phase Margin	ff	ff_min	-40	1.98	62.48	98.54	ss	ff_min	125	1.62	62.48	105.9
Phase Margin Frequency	ss	ff_min	125	1.62	554.3 K	21.57M	ff	ff_min	-40	1.98	554.3K	65.49 M
Vout	ss	ff_min	125	1.62	1.512	1.549	ff	ff_min	-40	1.98	1.512	1.565

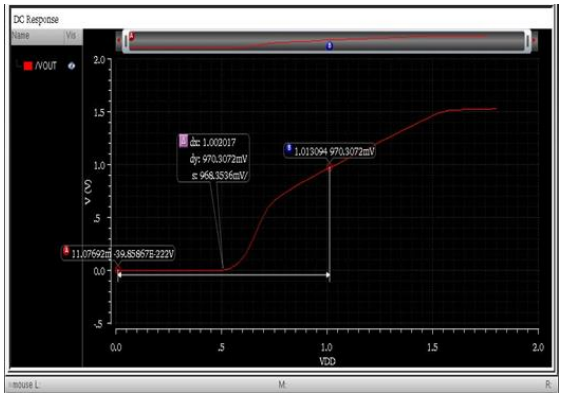

Fig. 12. Line Regulation

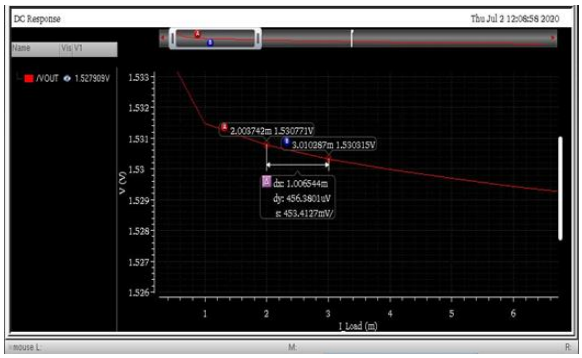

Fig. 13. Load Regulation

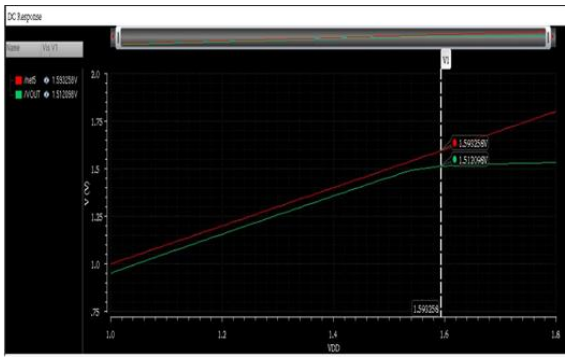

Fig. 14. Dropout Voltage

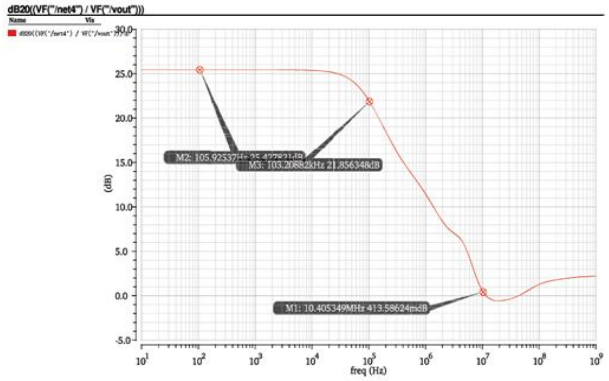

Fig. 15. LDO Overall Power Consumption

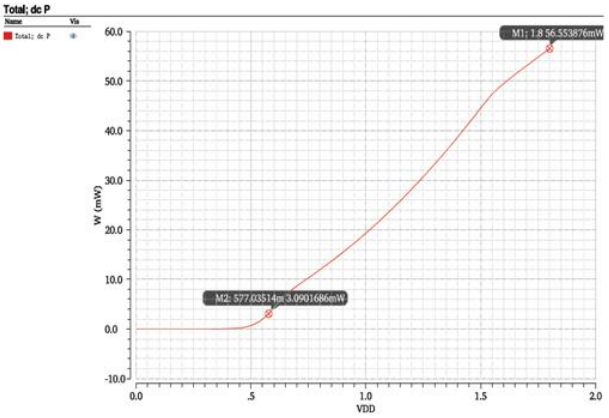

Fig. 16. PSRR (Power Supply Rejection Ratio)

6. Layout View

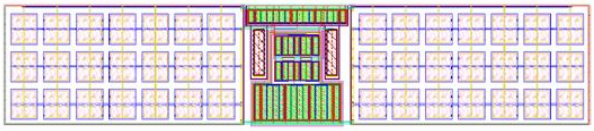
Fig. 17. Op-amp

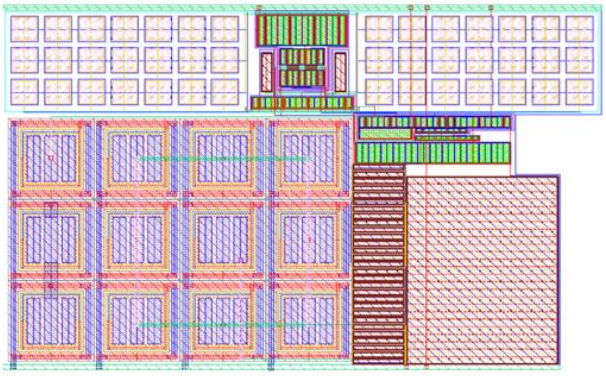
Fig. 18. Band Gap Reference (BGR)

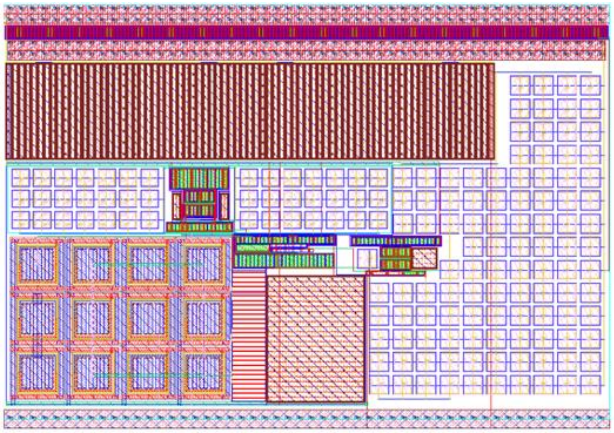

Fig. 19. Final LDO Layout

7. Conclusion and Future Scope

The circuit is designed in gpdk045nm CMOS technology with supply voltage of 1.8V and output voltage of 1.5V with reference voltage of 1.2V from BGR. Gain of the LDO system is obtained to be 16.98 dB at nominal condition and PSRR of 21.86@103KHz. The LDO system has a dropout voltage of 80mV with quiescent current of 390.802µA and the overall power consumption at full load of 30mA is 56.55339 mW.

A. Future Scope

Some suggestions and ideas for future work:

- From the continuous survey it is observed that the foundry of the technology and supply voltage range is continuously decreases with the advancement of technology. By scaling down the technology, we can get lower power consumption. We can designed a low power low drop-out regulator that is capable of delivering different output voltages, depending on the control signals.
- The operational trans-conductance amplifier (OTA) block can be improved using gain improvement techniques employed in the circuit, PSRR of the LDO can be improved.
- Improvement in Low Drop-out Voltage Regulator's slew rate can be achieved by using class AB amplifier at the output stage or by increasing the bias current. Sufficient slew rate improves the performance of the LDO.
- We can also design an ultra-low quiescent current low-dropout regulator with small output voltage variation and improved load regulation.

References

[1] Tiikkainen M, "LDO Voltage Regulator for On-Chip Power Management," University of Oulu, Department of Electrical Engineering. Master's Thesis, 86p. 2014.
[2] Paulo Crepaldi, Tales Pementa, Robson L. Moreno, "A CMOS Low Drop out Voltage Regulator". IEEE Conference 2010.
[3] Yogeshree Patil "Design and Analysis of Low Voltage Dropout Regulator (LDO)", IJSTE International Journal of Science Technology and Engineering Volume 1, 2015.
[4] Peijun Liu, S. Huang, Quanzhen Duan, Qian Zhu, and Zhen Meng, "A Low-Quiescent Current Off-Chip Capacitor-less LDO Regulator with UGCC Compensation", IEEE 2019.
[5] Qiang Li 1, Kai Wang, Jian-jun Zhao, Physics Department, Baotou Teachers College, Baotou, China, "A Capacitor-less LDO with Fast transient response using Push-Pull Buffer", IEEE, 2019.
[6] Hongguang Zang, Zhangwen Tang State Key Laboratory of ASIC & System Funda University Shanghai, "A 318 nA Quiescent Current 0-10mA Output Transient Enhanced Low-Dropout Regulator Applied in Energy Harvest System", IEEE, 2017.
[7] Behnam Samadpoor Rikan, Hamed Abbasizadeh, Truong Thi Kim Nga, Sung Jin Kim and Kang-Yoon Lee College of Information and Communication Engineering Sungkyunkwan University Suwon, South Korea,"A Low Leakage Retention LDO and Leakage-based BGR with 120nA Quiescent Current", IEEE 2017.
[8] Xudong Liang, S. Huang, Quanzhen Duan, Yue min Ding, and Kailiang Zhang, A 802 nA Quiescent Current and 100 mA Load Low-Dropout Regulator for Micro Energy Harvest System", IEEE, 2018.
[9] Gabriel Alfonso Rincon-Mora and Phillip E. Allen, "Study & Design of Low Drop-Out- Regulators."
[10] Vijay Kumar Peddinti, "ELE539 Project Band-Gap Reference Circuit."