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Energy Efficient Successive Approximation Based ADC

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***Abstract*: In today's electronic industry power efficient Successive approximation Analog-to-Digital converter (SAR ADC) architecture is widely used, it is very compact compared to other ADC's architecture. In this proposed design practical implementation of 10-bit SAR-ADC is done using HDL. The SAR block uses a binary search algorithm for convenient conversion. The SAR-ADC is implemented using 180nm technology as a result this topology shows low power consumption.**

***Keywords*: Binary search, Design methodology, HDL language, SAR-ADC circuit, Track and hold circuit.**

1. Introduction

Analog-to-Digital converters (ADC's) are the key building blocks between the analog and digital domains, the invention of high-performance chips is very important in real world VLSI technology. The performance of the whole system is often constrained by ADC's they play an important role in many mixed-signal systems. Due to the prevailing applications of green electronics, consumer electronics and biomedical applications, low power consumption has become a critical and essential target.

The generalized symbolic representation of Analog-To-Digital converter block is as shown,

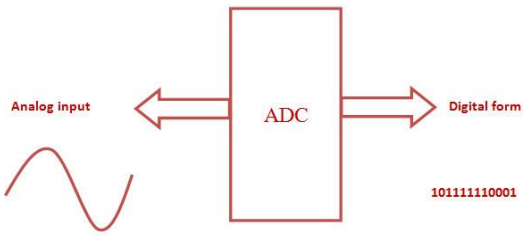

Fig. 1. Analog-to-Digital Converter

Fig. 1, translates analog signal to digital language with a tradeoff between power consumption and speed. Among the various architecture of ADC's, the Successive Approximation Register (SAR) ADC has attracted more attention in the recent years due to its excellent power efficiency and suitability for Medium-to-high-speed applications.

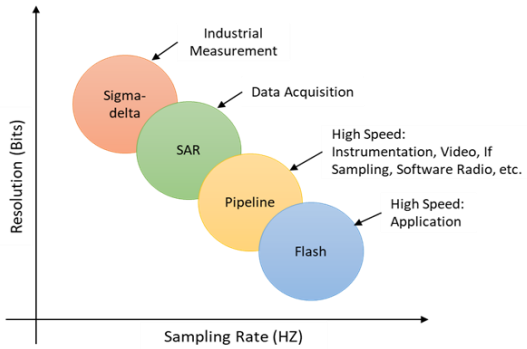

Fig. 2. Types of ADC's

Common types of ADC have for different application is categorized as shown in Fig. 2.

In this paper the design of low power Successive approximation ADC is proposed. [1] Successive approximation ADC architecture was first implemented by Bernard M. Gordon. SAR ADC'S have decent conversion speeds (about 50Hz to 4MHz) [2]. They also take a small overall chip area in comparison to flash ADC [5]. This converter design also goes well with the use of serial output port due to the conversion method. The power consumption is further reduced than [3]. SAR logic can be designed from [4]. The overall SAR ADC architecture is analyzed and verified.

2. Objectives

- The SAR-ADC is an Analog-to-Digital converter which uses Successive Approximation technique.
- The low power consumption and reduction in overall net area are the main vision of this venture.
- Since SAR-ADC's are widely used in all sorts of electronic device applications, low power consumption becomes a vital parameter.

3. Design implementation

A. *Operation of SAR-ADC*

The SAR-ADC works by many built-in circuits such as the Track and hold circuit, Comparator, SAR block etc.

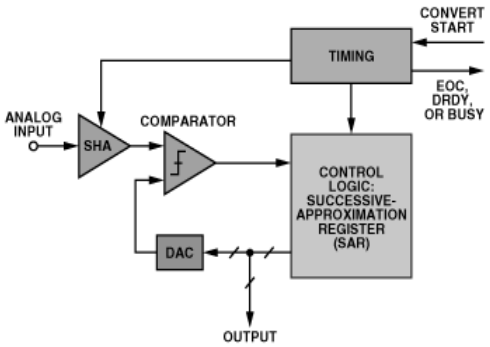

Fig. 3. Block diagram of SAR-ADC

1) Track and hold

During the process the conversion cycle analog input is given to the Track and hold circuit (T/H) to keep the signal constant. It samples the input and holds till the falling edge of the clock pulse.

2) Comparator

Comparator block compares the signal from the (D/A) and the sampled signal. The resultant most-significant bit (MSB) is 0 or 1 is stored in SAR.

3) Successive Approximation Register (SAR)

The complete conversion takes place at the SAR, the SAR follows an algorithm called binary search algorithm. The SAR

Algorithm works by switching on a large voltage and comparing that to the input voltage. If the switch voltage proves higher than the input voltage it keeps that voltage on. This corresponds to 1's and 0's.

4) Requirements and specifications

One, it needs high accuracy over the sampling speed range seeing so the customer receives accurate data.

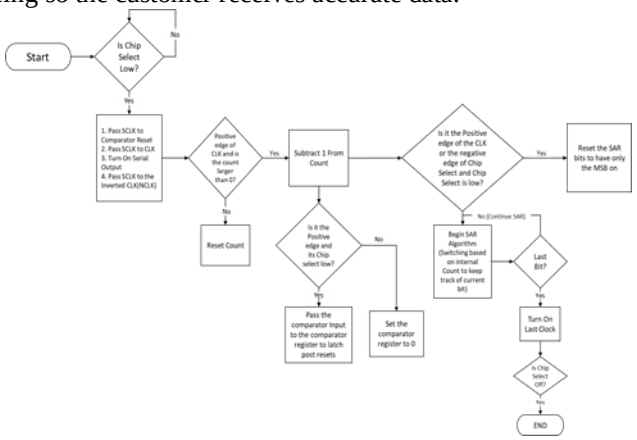

Fig. 5. Flow chart

Two, it needs comparable resolution to what comes standard on the development boards currently on the market to provide an effective alternative. Third, due to the constraints already put on the technology that it uses the size needs a specific limitation, which nicely coincides with keeping it compact for the consumer. Using a serial interface makes sense for this design and SPI has a limit of 10 bits on most micro-controllers [6] so this sets the largest resolution that the ADC can output. Table I addresses the consumer needs and puts them in terms of marketing requirements and engineering specifications.

4. Methodology

This section breaks the design down into 3 separate levels. Level 0 depicts a basic block diagram showing all of the inputs and outputs of the ADC. Level 1 depicts the basic flow of the signals in the design and how the signal processing works. Level 2 shows all of the connections made in the chip and how everything interacts with each other.

Fig. 4. Level 0 diagram

Fig. 4, shows the level 0 block diagram. It has 5 inputs and 1 output with 3 of the inputs controllable externally (Chip Select, Serial Clock, and Analog Input).

1.8V Power Supply: DC power supplied from external source. (I.e. micro-controller or battery)

Analog Input: Input coming from sensor in the analog domain with a 0V to 1V range.

Chip Select: This control signal tells the ADC that it needs to operate and use the SPI line.

Serial Clock: External SPI clock taken from the controller to act as the base clock for the ADC

Outputs: Serial Output Digital code sent out by the ADC representing a voltage value to desired data storage location.

Digital Controls:

The digital controls make up the brain of the ADC. It tells all the different analog components when to turn on and off based on a set flow. In this case that flow comes from the Successive Approximation Algorithm, Fig. 5 shows a simple flow diagram showing the basics of how design's code works. All diamond shapes make up decisions and all squares make up processes based on a set flow.

5. Results and Discussions

The main contribution to this work is low power consumption. The 10-bit SAR ADC is designed in the front-end using cadence and the power and area are analyzed. The net list is generated and designed is mapped. The reduction in power consumption than the existing design is shown below.

The overall net area was found to be 1411 nm and the total power consumption of the work was 29743.53 nW.

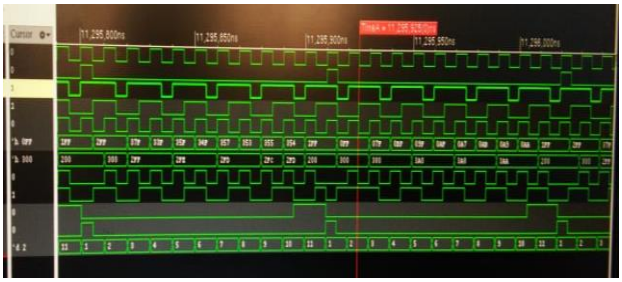

Fig. 6. Waveform of complete SAR ADC

Table 1
Comparison results of SAR ADC output for 10-bit resolution

Serial no	[7]	Proposed work
Power consumption (micro watts).	265	29.73
Total area (nm)	1485	1411
Resolution	10	10
Supply voltage	1.8	1.8

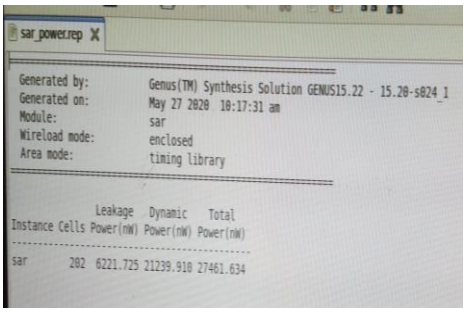

Fig. 7. Power consumption of SAR-ADC

6. Conclusion

The SAR ADC is implemented in 180 nm technology using cadence and low power consumption is achieved. The area was also calculated and a cost-efficient methodology is applied.

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