International Journal of Research in Engineering, Science and Management
Volume-3, Issue-6, June-2020
www.ijresm.com | ISSN (Online): 2581-5792

Design and Development of 7-Level Multi-Level Inverter

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***Abstract*: Recently, almost all industrial devices are mostly build on electronics devices which are precisely sensitive to harmonic. In order to meet the requirement from the industries demand aimed at a free-harmonics and high power rating source is remarkably increased in past few years. An inverter which a device or electric circuit that convert DC to AC is one of the electronic devices that gives concern for implementing of generating a neat power source. The main focus of this project is to improve the efficiency of MLI and to improve the quality of the output waveform and reduce the number of switches. Seven level reduced switches topology has been implemented with seven switches. We use for elimination of harmonics is THD (total harmonics distortion) method. Selective harmonics elimination and fundamental stepped waveform (SHESW) method is implemented to eliminate the lower order harmonics.**

***Keywords*: THD (Total harmonic distortion), multilevel inverter (MLI), SHESW (selective harmonics elimination stepped waveform).**

1. Introduction

A multilevel inverter is a power electronic device which converts the lower level dc voltage into desired alternating voltage. A Multi-level inverter is used in order to generate the AC voltage from DC voltage. Multilevel converters are mainly utilized to synthesize a desired single voltage waveform. The desired multi-staircase output voltage is obtained by supply. Multilevel inverters continue to receive more and more attention because of their high voltage operation capability, low switching losses, high efficiency and low output of Electro Magnetic Interference (EMI). Nowadays, multilevel inverters are becoming increasingly popular in power applications, as multilevel inverters have the ability to meet the increasing demand of power rating and power quality associated with reduced harmonic distortion.

The most attractive features of a multilevel inverter are as follows:

1) They can generate output voltages with extremely low Distortion and lower dv/dt.
2) They draw input current with very low distortion.

2. Multi-level Inverter

In recent years the Multi-Level Inverters are very popular for Industrial and powers system applications due to their advantages on two-level inverters i.e. High Power rating, Low Harmonics so they give the higher efficiency. The different topologies of Multi-Level Inverters are Neutral-point clamped (NPC) or Diode Clamped (DC) inverter, Flying capacitor inverter and Cascade inverter. As the level increases, NPC require more clamping diodes so the control of real power flow becomes very difficult. In flying capacitor inverter as the level increases, number of storage capacitors also increases hence they becomes bulky and costly; there are more switching losses in this topology. A 7-level MLI was generated with 9 switches reducing 3 switches from the main conventional CMLI. It offers good results yielding desired a 7-level output with low THD.

3. Block diagram of Multi-Level Inverter

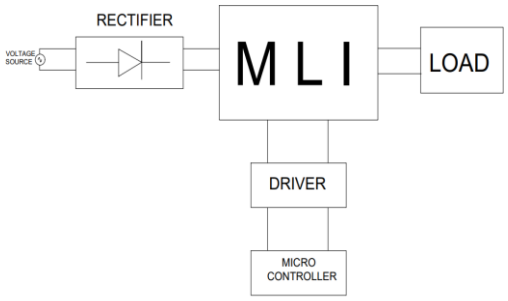

Fig. 1. Block diagram of multi-level inverter

The block diagram of Multilevel Inverter. It consists of rectifier whose output is fed to MLI and the output of MLI is fed to Induction Motor. Driver circuit is used to boost voltage and current. 7-Level, 5 Switches. It consists of 4 dc sources of 7 levels, the proposed 7 level MLI is about redesigning of existing 6-switch topology eliminating 1 switch attaining the tag of 5 switch configuration. The circuit thus obtained is the simplest design compared to conventional and all other existing topologies.

4. Multi-Level Inverter Circuit

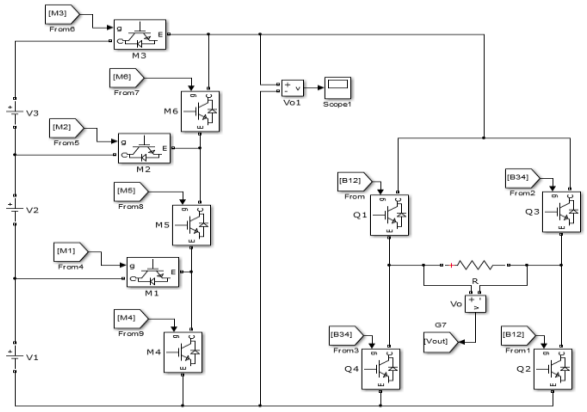

Fig. 2. Circuit diagram of multi-level inverter

The circuit is in the form of H-bridge type network. On the left hand side circuit diagram is consist of six MOSFETS which have connected through voltage sources.

This circuit is auxiliary circuit which is used to boost the voltage level signals of the circuit. The right hand sided circuit is H-bridge which is used for polarity shift of cycles. This circuit have variable resistance to measure the output across it. An H-bridge is built of four switches that control the flow of current to a load. ... If you close switch 1 and switch 4, the current will flow from the source, through switch 1, and then through the load, then through switch 4, and then back to the load. An H-bridge circuit with S2 and S3 closed. The H-bridge arrangement is generally used to reverse the polarity/direction of the motor, but can also be used to 'brake' the motor, where the motor comes to a sudden stop, as the motor's terminals are shorted, or to let the motor 'free run' to a stop, as the motor is effectively disconnected from the circuit.

5. Input Signal of the Multi-Level Inverter

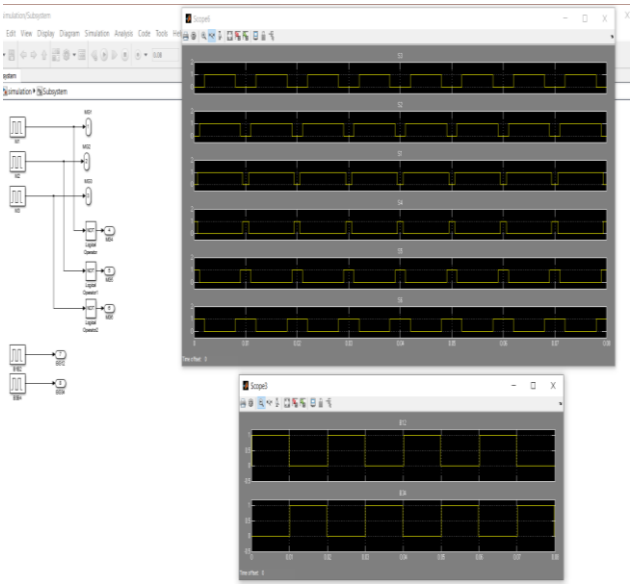

Fig. 3. Input signal of multi-level inverter

As input signal is applied to the multi-level inverter circuit as shown in fig. 3. The circuit is consists of six switch and generated pulses by using the voltage. The first three switch will be the positive cycles then next three will be negative cycles this is applied in MATAB SIMULATION. By giving a NOT operation after the three switch it will convert to the negative cycles. Then next two waveforms are used for polarity operation of the waveform. This is used under the H-bridge operation. The first diagonal switch is generated positive cycle then next diagonal switch is generated negative cycle. A NOT gate, often called an inverter, is a nice digital logic gate to start with because it has only a single input with simple behavior. A NOT gate performs logical negation on its input. In other words, if the input is true, then the output will be false. Similarly, a false input results in a true output.

6. Total Harmonic Distortion

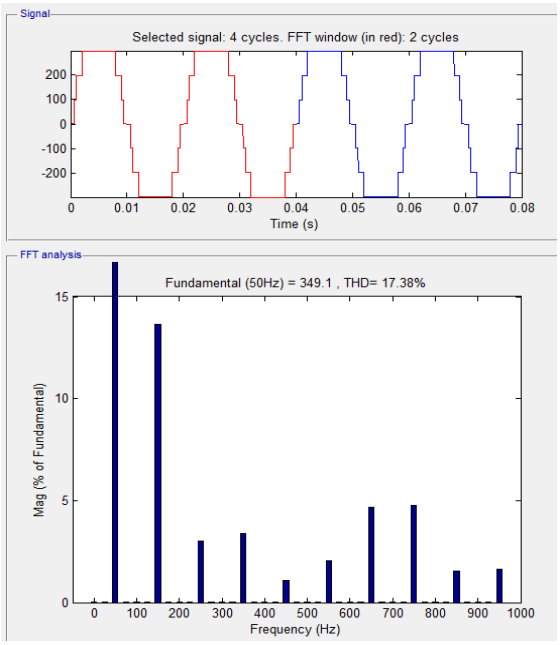

Fig. 4. Total harmonic distortion of multi-level inverter

In this circuit total harmonic distortion (THD) is obtained in SIMULATION is 17.38%. Harmonics are unwanted higher frequencies which superimposed on the fundamental waveform creating a distorted wave pattern. In an AC circuit, a resistance behaves in exactly the same way as it does in a DC circuit. That is, the current flowing through the resistance is proportional to the voltage across it.

7. Equal Phase Method

The equal phase method calculation is:

Equal Phase Method (EP Method):

$a1 = I * 180^0 / M$

Where I = 1, 2... (M-1)/2

M = Level of Output Voltage (7)

Calculation to find angle (a):
a1 = 1 * 180^0 / 7 = 25.71
a2 = 2 * 180^0 / 7 = 51.42
a3 = 3 * 180^0 / 7 = 77.13
Calculation to find time delay:
Example for delay 1:
For 360^0 the time delay taken is 0.01sec (changeable)
For 25.71^0 we get 0.00071sec
This method is used to find the delay time and the switching angle.

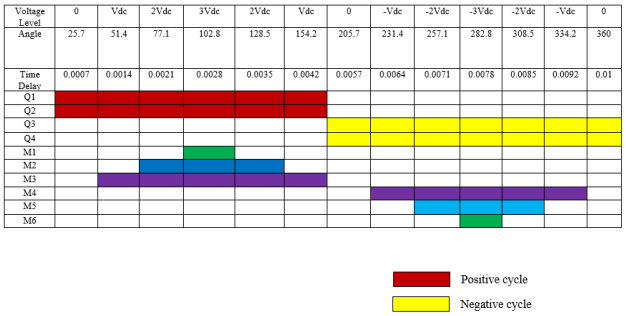

Fig. 5. Chart of delay time and switching angles

In the above fig-5 we can observe the switching angle and delay time for the 7 level multi-level inverter. And the switching operations is also showed in the table.

8. Output waveform

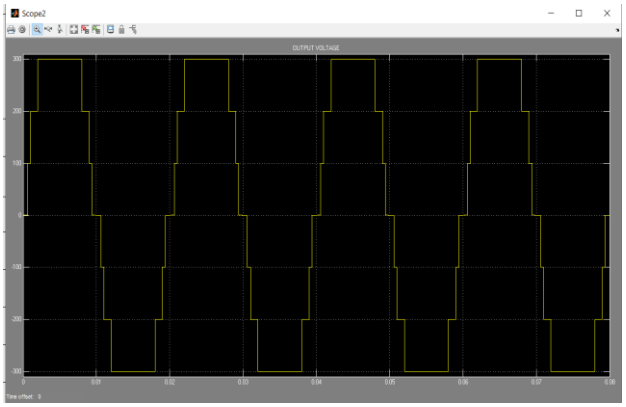

Fig. 6. Output waveform of 7 level multi-level inverter

The output of the 7 level multi-level inverter is shown in the fig. 6.

9. Hardware Circuit of MLI

In the hardware circuit we use active and passive components. The apparatus are resistors, capacitors, MOSFET, opto coupler, microcontroller, diodes, transformers and output as motor with no load.

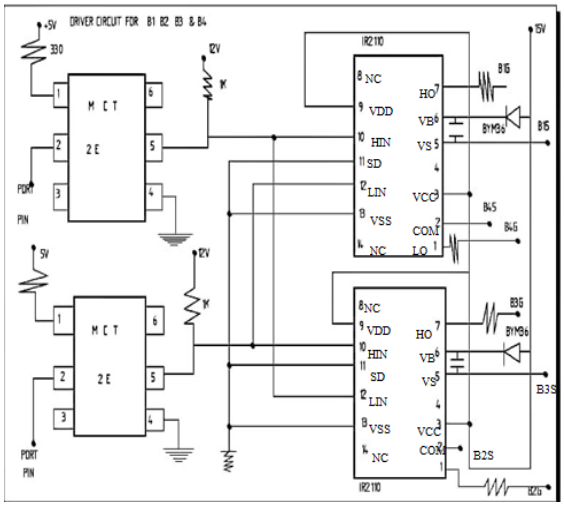

Fig. 7. Hardware circuit of 7 level multi-level inverter

10. Applications

- Motor drives.
- Electric vehicles drives.
- DC power source utilization.
- High voltage system.
- Interfacing with renewable energy resources.
- Back to back frequency link system.

11. Advantages

- Switching losses is reduced.
- High switching frequency up to 10 KHz.
- Reduced harmonic distortion.
- Switching frequency.

12. Disadvantages

- Large numbers of capacitors are bulky and more expensive than the clamping diodes used in the diode-clamped multilevel inverter.
- Every H-bridge needs a separate DC source.

13. Conclusion

- The 7-level MLI using just 6 switches is successfully introducing, simulating the circuitry using SIMULINK, the main idea of the configuration is to reduce the number of power device.
- The technique can generate stepped waveforms with a wide range of modulation indices, as well as minimized number of power device and harmonic distortion.
- The system will be modeled and suggested the suitable 7 level output.

References

[1] I. Colak, R. Bayindir and E. Kabalci, "Design and analysis of a 7-level cascaded multilevel inverter with dual SDCSs," SPEEDAM 2010, Pisa, 2010, pp. 180-185.