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Power and Delay Analysis of Different SRAM Techniques

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***Abstract*: In recent years the demand for low power devices have been increases tremendously. To solve the power dissipation problem, many researchers have proposed different ideas from the device level to the architectural level and above. The demand for static random-access memory (SRAM) is increasing with large use of SRAM in System On-Chip and high-performance VLSI circuits. This paper represents the simulation of different SRAM cells and their comparative analysis on such as Average Power and the performance(Delay). All the simulations have been carried out on "Pyxis" 180nm and 130nm technology at "Mentor Graphics" tool.**

***Keywords*: VLSI, SRAM, Delay, Power.**

1. Introduction

SRAM based cache is most vital element of VLSI chip. The speed and power of overall system is disserted peripheral circuit the delay in reading is the most concern in the designing of SRAM cache after latching process the current flow stops automatically. The term memory is usually used as a short hand for physical memory which refers to the actual chips capable handling data. CMOS devices have been scaled for high performance and high density. High performance can be achieved by reducing the supply voltage and parallelly reducing threshold voltage. SRAM are used in cache memory which needs to be very fast, robust and have less area [2]. The transistors have been lowered which also contributes to leakage currents and reduces the battery life dramatically. Solutions involving additional transistors, i.e.,8T, and 9T, 10T, Differential 10T have been explored to lower power consumption while reducing these adverse effects in the cell performance. Therefore, considerable attention is given to minimize the leakage power SRAM cell. Tradeoff between speed and leakage power is discussed in [3], lowering the threshold degrades the performance, and increasing threshold increases line leakage, cell leakage and lower cell stability. Cell stability depends up on the threshold voltage. In this paper SRAM Cells topologies that allow the analysis and simulations of different parameters at 180nm and 130nm technology successfully on the basis of the, average power and performance(delay) with the area efficiency of the circuit.

2. Implementation

This section discusses about the implementation of different SRAM cells.

A. 6T SRAM cell

The conventional circuit of one bit SRAM cell consists of 6 MOSFETs. In SRAM there are three modes of operation. i.e., read write, hold. The schematic diagram of 6T SRAM cell is shown in Fig. 1. Access to the cell is enabled by the word line (WL) which controls the two access transistors, in turn, control whether the cell should be connected to the bit lines: BL and BLB. They are used to transfer data for both read and write operations.

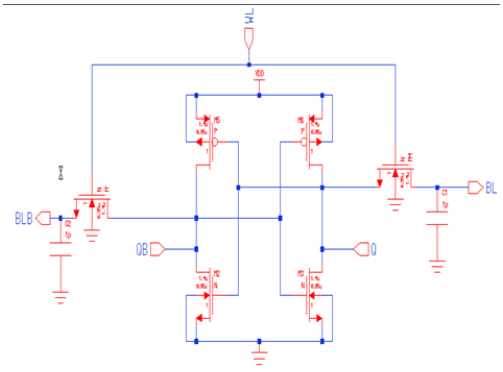

Fig. 1. Schematic of 6T SRAM cell

B. Read Operation

Read phase BL and BLB are precharged to V_{dd} and then WL is made high such that the transistors M2 and M3 turns ON. For read '1' BLB gets discharged to ground through the M4 transistor. BL is not discharged and remains in V_{dd} since the M1 transistor is OFF.

C. Write Operation

For write operation BL is charged '1'or down to '0' regarding the data to be stored. BLB is charged by inverted voltage of the bit line (BL). To write '1' BL is charged to V_{dd} and WL is made high such that the current passes through M2 and M3 transistors and '1' gets stored in node Q through M2 and

M3 and '0' stored in the node QB, which makes the transistors M5 and M4 ON. To write '0' BL is retained at ground and BLB is charged to V_{dd} so that '0' is stored at Q and '1' at QB.

D. 8T SRAM cell

Through upsizing, the SRAM cell can operate at very low supply voltages (i.e. low V_{DDmin}) with minimized threshold voltage variation with a penalty of increased area. However, continuously increasing process variations in 180 nm and 130 nm technologies has led to a pronounced degradation in stability of SRAM cells especially at lower voltages. To overcome this issue, extra two transistors are added by making transistor count 8. Proposing a new SRAM cell to improve both read and write margins under scaled supply voltages is crucial for ultra-low power applications with low penalty on area, access time, and leakage power consumption.

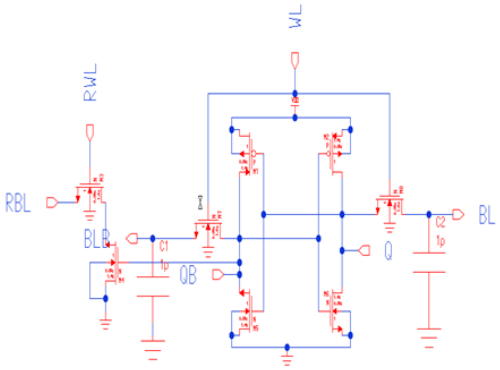

Fig. 2. Schematic of 8T SRAM cell

The proposed 8T-SRAM cell where two transistors, one NMOS and one PMOS are added to the standard 6T-SRAM cell while the mechanism of read is single-ended. During read, only RWL is asserted while during write both WL and RWL signals are set to high. There are separate read word line and write word line for read access and write access. Read access is done through newly added two transistors and write access is done similar to 6T-SRAM cell. In 8T-SRAM cell, read bit line leakage is large so it is impossible to design higher memory using 8T-SRAM cell.

E. 9T SRAM cell

A 9T SRAM cell is proposed is to reduce both bit line leakage and cell leakage. Schematic of 9T SRAM cell is shown in the Fig.3.This circuit shows reduced leakage power and enhanced data stability. The 9T SRAM cell completely isolates the data from the bit lines during a read operation. The idle 9T SRAM cells are placed into a super cutoff sleep mode, thereby reducing the leakage power consumption as compared to the standard 6T SRAM cells.

9T SRAM cell considering stability, energy consumption and delay. A write bit line balancing scheme is proposed to reduce the leakage current of the SRAM cell. A 9T structure is to improve the SNM by separating the read access structures of the original 6T cell, thus making the read SNM equal to the hold SNM. An innovative precharging and bit line balancing scheme for writing operation of the 9T SRAM cell is also proposed for maximum standby power savings in an SRAM array.

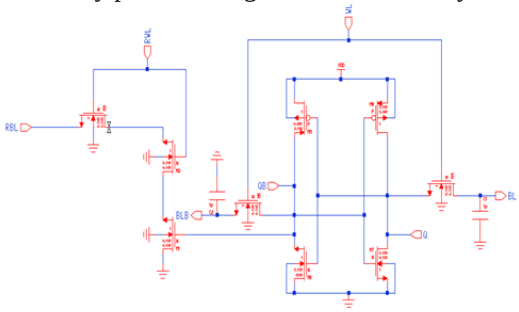

Fig. 3. Schematic of 9T SRAM cell

F. 10T SRAM cell

To address the problem of designing higher memory new 10T cell is proposed. In 10T SRAM cell one extra PMOS is added to prevent the line leakage by keeping the node high. The schematic of 10T SRAM cell is shown in fig. 4.

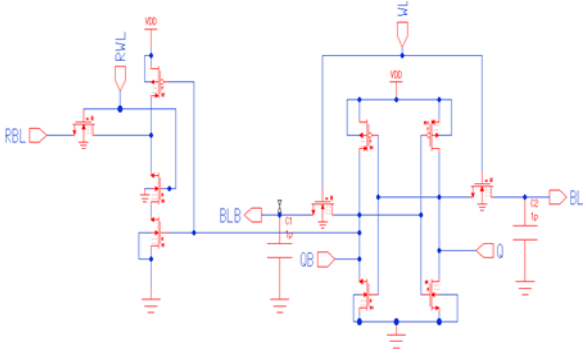

Fig. 4. Schematic of 10T SRAM cell

By using this cell, we can design higher memory, however extra leakage current flowing through PMOS will increase the standby power consumption.

3. Simulation results and comparison

Read Analysis of 6T SRAM cell

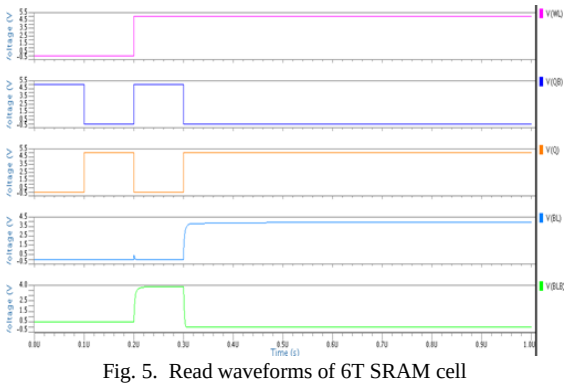

Fig. 5. Read waveforms of 6T SRAM cell

Write Analysis of 6T SRAM cell

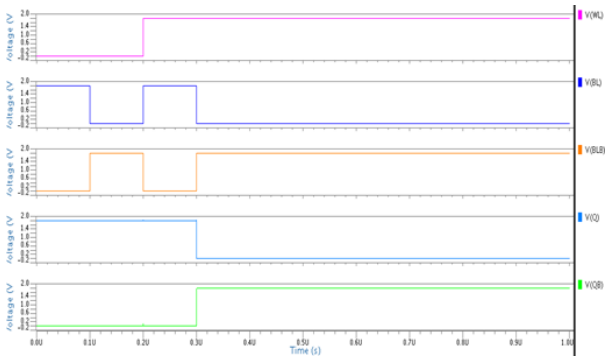

Fig. 6. Write waveforms of 6T SRAM cell

Read Analysis of 8T SRAM cell

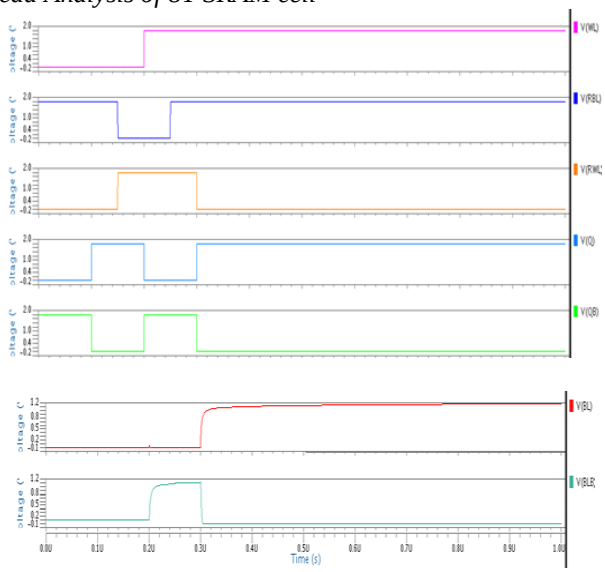

Fig. 7. Read Waveforms of 8T SRAM cell

Write Analysis of 8T SRAM cell

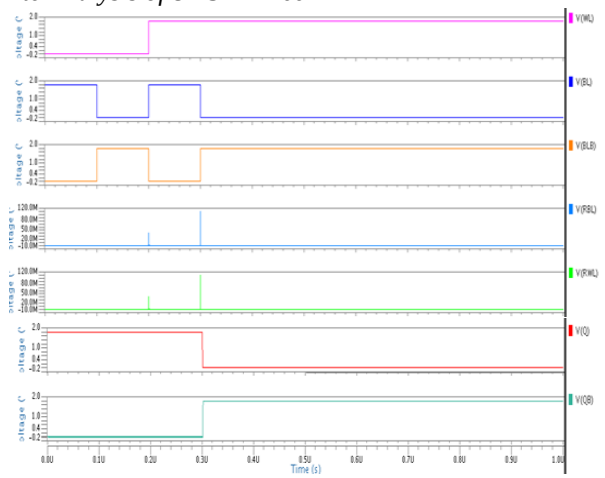

Fig. 8. Write Waveforms of 8T SRAM cell

Read Analysis of 9T SRAM cell

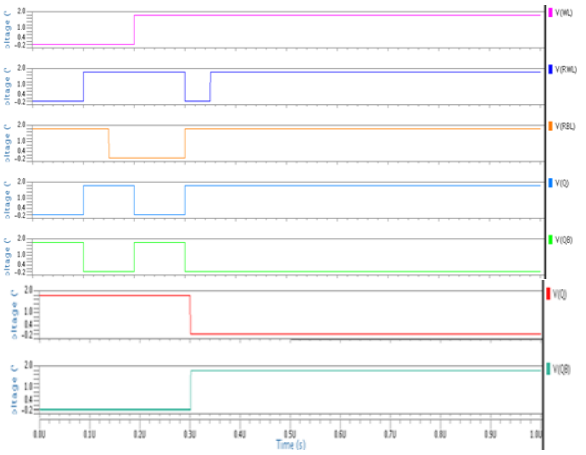

Fig. 9. Read Waveforms of 9T SRAM cell

Write Analysis of 9T SRAM cell

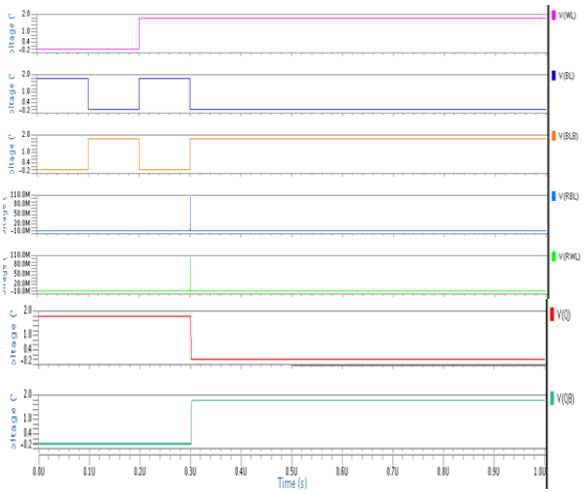

Fig. 10. Write Waveforms of 9T SRAM cell

Read Analysis of 10T SRAM cell

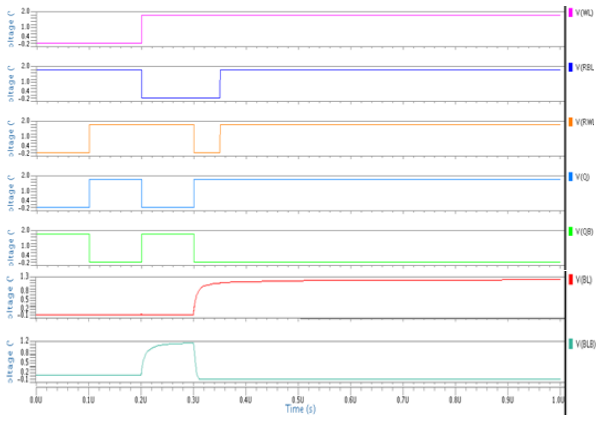

Fig. 11. Read Waveforms of 10T SRAM cell

Table 1
Comparison Table

Parameter		180nm		130nm	
		Delay	Power	Delay	Power
6T	idle	18.465n sec	218.79n W	100.78n sec	1.616u W
	read	1.2372n sec	6.090m W	633.74 p sec	459.29 u W
	write	100.29 n sec	183.36 n W	155.41 p sec	285.27 n W
8T	idle	55.334 n sec	29.134 u W	100.25 n sec	726.02 n W
	read	103.53 n sec	30.815 u W	100.78 n sec	1.7030 u W
	write	103.31 n sec	190.33 n W	182.67 p sec	290.02 n W
9T	idle	118.45 n sec	125.01 u W	50.898 n sec	2.5285 m W
	read	108.99 n sec	5.859 u W	456.77 p sec	2.5285 m W
	write	542.39 p sec	387.54 n W	182.67 p sec	290.02 n W
10T	idle	143.80 n sec	115.48 u W	456.80 p sec	3.4130 m W
	read	108.44 n sec	17.313 m W	50.895 n sec	3.4130 m W
	write	398.95 n sec	414.04 u W	100.15 n sec	287.14 n W

Write Analysis of 10T SRAM cell

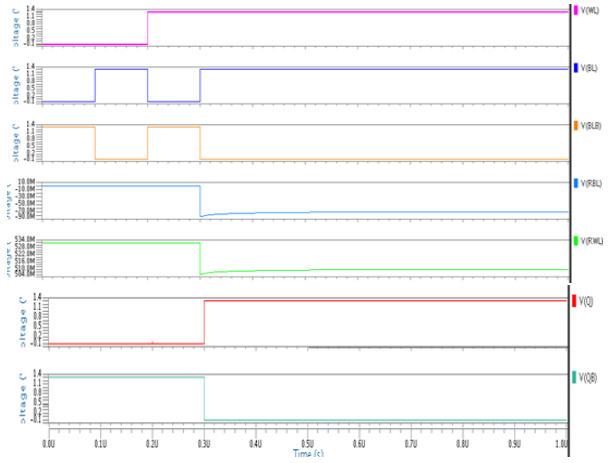

Fig. 12. Write Waveforms of 10T SRAM cell

4. Conclusion

In this paper all the four SRAM structures are analyzed successfully. The problem of read SNM of conventional 6T SRAM cell are solved using 8T SRAM Cell. 8T SRAM cell is very good for low dense memory but using 8T SRAM cell we cannot make it high dense memory due to high bit-line leakage.10T SRAM cell is made for building higher memory but it has more standby leakage current due to PMOS. 9T SRAM cell is better but it has a penalty of little bit more area. It saves more power as compared to10TSRAMcell.

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References

[1] Jawar Singh, Dhiraj K. Pradhan," A single ended 6T SRAM cell design for ultra-low voltage applications", IEICE Electronic Express, 2008, pp. 750-755.
[2] Kang, Sung-Mo, Leblebici and Yusuf (1999), "CMOS digital integrated circuits analysis and design", McGraw-Hill International Editions, Boston, 2nd Edition.
[3] C. T. Chu, X. Zhang, L. He and T. Jing, "Temperature aware microprocessor floor planning considering application dependent power load", in Proc. of ICCAD, 2007, pp. 586-589.
[4] Narender Hachette and Nagarajan Ranganathan, "LECTOR: A technique for leakage reduction in CMOS circuits," IEEE Trans., on VLSI Systems, vol. 12, No. 2, Feb. 2004.
[5] Chang, L. Montoye, R. K. Nakamura, Y. Batson, K. A. Eickemeyer, R. J. Dennard, R.H. Haensch, W. J. amsek, D, "An 8T-SRAM for variability tolerance and low-voltage operation in high performance caches", Solid-State Circuits, IEEE Journal, vol. 43, April 2008, Issue 4, pp. 956-963.