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Low Noise Amplifiers Designs: A Review

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***Abstract*: The accuracy of low frequency noise measurement has been concerned because it is an important technique for evaluating the reliability of components. LNA design is very difficult work in the receiver part because the signal which received is very weak and gets affected easily with the noise. Therefore, it is necessary that new design must give noise figure as low as possible over a wide range. Its simulation based analysis is also important to test its stability and performance before fabrication. As it is difficult to get all the characteristics of LNA perfectly therefore there is always a tradeoff between gain and noise. The analysis concerns different design structures and it is carried out using the Advanced Design Simulator (ADS) software of Agilent Technologies Inc.**

***Keywords*: LNA-Low Noise Amplifier, NF-Noise, S11-input return loss, S22-output return loss, Gain-S21.**

1. Introduction

A low-noise amplifier (LNA) is an electronic amplifier that amplifies a very low power signal without significantly degrading its signal-to-noise ratio. An amplifier will increase the power of both the signal and the noise present at its input, but the amplifier will also introduce some additional noise. LNAs are designed to minimize that additional noise. Designers can minimize additional noise by choosing low noise components, operating points, and circuit topologies. Minimizing additional noise must balance with other design goals such as power gain and impedance matching.

LNAs are found in radio communications systems, medical instruments and electronic test equipment. A typical LNA may supply a power gain of 100 (20 decibels (dB)) while decreasing the signal-to-noise ratio by less than a factor of two (a 3 dB noise figure (NF)). Although LNAs are primarily concerned with weak signals that are just above the noise floor, they must also consider the presence of larger signals that cause inter modulation distortion. An LNA is a key component which is placed at the front-end of radio receiver circuit. The LNA is needed because the received signal is weak. The received signal is usually a little above background noise. Satellites have limited power so they use low power transmitters. Low-noise amplifiers are a significant part of a receiver circuit whereby the received signal is processed and converted into information. LNAs are designed to be close to the receiving device so that there is minimum loss due to interference. As the name suggests, they add a minimum amount of noise (useless data) in the received signal because any more would highly corrupt the already weak signal. When the signal-to-noise ratio (SNR) is high and needs to be degraded by around 50 percent and power needs to be boosted, an LNA is used. An LNA is the first component of a receiver to intercept a signal, making it a vital part in the communication process.

2. Literature survey

A. Different technologies used to design LNA

1) FET-BJT technologies

[2] The NF performance is around 1.6 dB, the current consumption for this LNA is 2.0 mA for a 2.7 V supply voltage VCC.

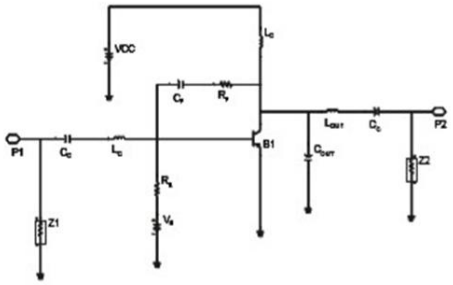

Fig. 1. Bipolar SiGe LNA

[4] 10 GHz is designed with a noise figure less than 3 dB and gain more than 9 dB along with input and output reflection coefficients less than –10 dB.

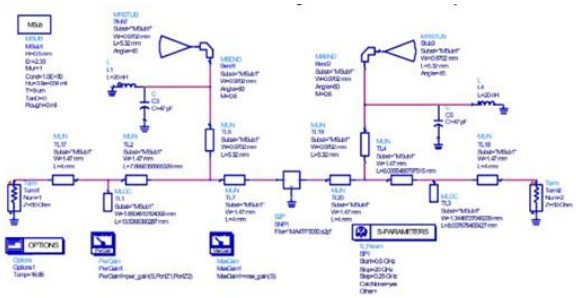

Fig. 2. ADS schematic diagram of the proposed 10 GHz LNA

[5] Gain flatness less than 1dB and noise figure is between 1.9 - 2.3dB at 0.5 -6GHZ, achieved 30 - 28.5 dB at 0.5 – 6 GHz

gain (S21), Output reflection coefficient is -10 dB at 6ghz.

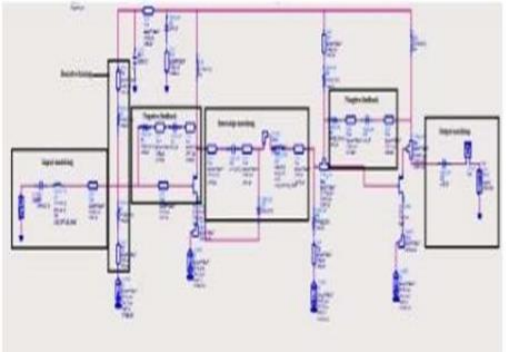

Fig. 3. Schematic for 0.5GHz to 6 GHz UWB Low Noise Amplifier

[7] At l.0 GHz, the proposed BJT-LNA has a low noise figure (NF) of 0.359dB, with input return loss of 6.022dB, output return loss of 1.447dB and a voltage gain of 3.296dB.

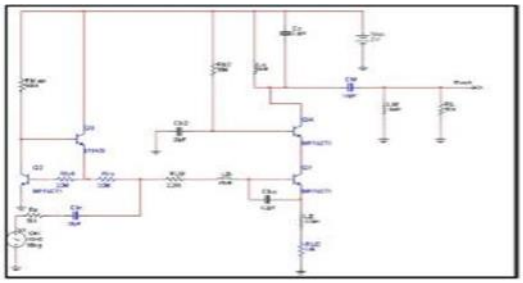

Fig. 4. Complete Schematic of the 1.0GHz BJT-LNA

[8] Achieves 1.3 dB NF, 15 dB gain, 55 dB isolation, and +10 dBm IIP3 with 2.5 mA of collector current at VCE = 1.5 V.

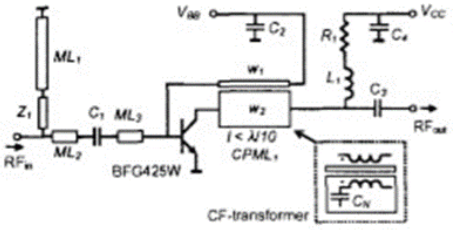

Fig. 5. Circuit design of 900 MHz CECF LNA

[18] The average noise coefficient is 12.537, the average noise coefficient from low noise amplifier three amplifying circuit is designed for 12.654.

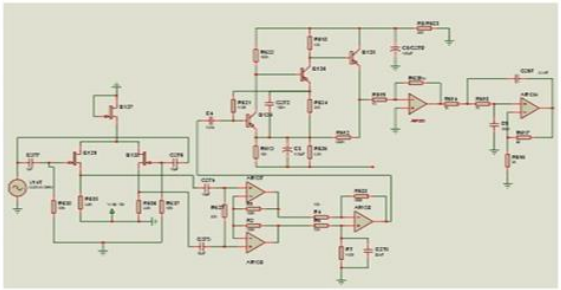

Fig. 6. Low Noise Amplifier at 4.6Hz-91.2KHz

[14] In the frequency of 2.4GHZ, the input VSWR is 1.460dB and the output VSWR is 1.501dB. In the frequency of 2.2GHz-2.6GHz, the VSWR of some point are much bigger than 1.5dB.

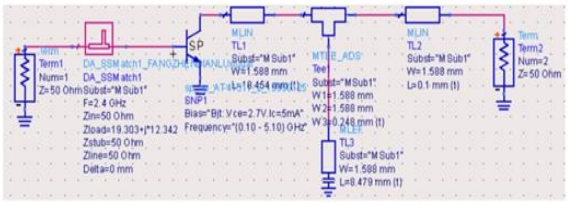

Fig. 7. The SP model circuit

[15] The input and output return losses were better than 11 dB and 19 dB, respectively, noise figure of less than 1.4 dB

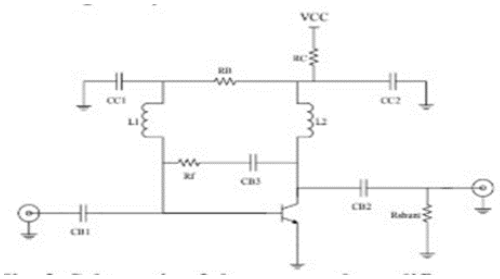

Fig. 8. Schematic of the proposed amplifier

[17] Noise figure of 1dB with a flatness of 0.5 dB and input output return losses better than -15dB have been achieved over 100MHz bandwidth.

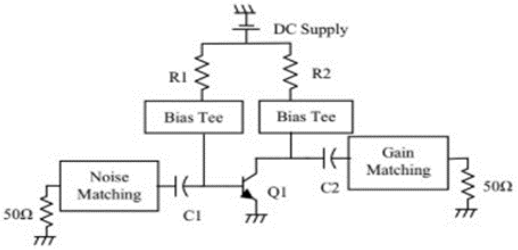

Fig. 9. Circuit diagram of single stage LNA

2) CMOS-technologies

[1] LNA design (3-5 GHz) in 130 nm CMOS technology. Simulation results showed a minimum noise figure (NF) of 2.3 dB, max gain 9.6 dB and 0.25 mW power dissipation.

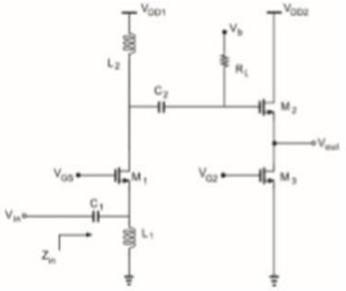

Fig. 10. CG LNA

[9] LNA can achieve power flat gain of 10dB with input matching of -9.76dB; the minimum noise figure 3.7dB; and input third-order-intercept point (IIP3) of -1dB. The power dissipation is only 7.2mW.

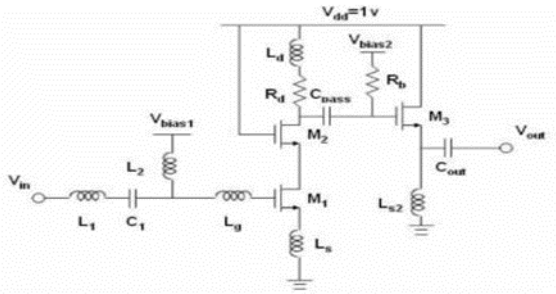

Fig. 11. Schematic of the UWB LNA

[10] Achieve power gain over than10dB at 5.8GHz.

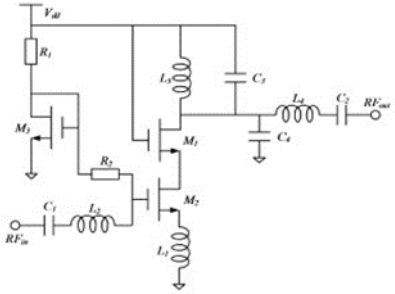

Fig. 12. Circuit schematic of LNA

[11] 12.4dB power gain, 4.2dB noise figure, -5.0dBm output P1dB and 5.6dBm OIP3 with 15.5mW.

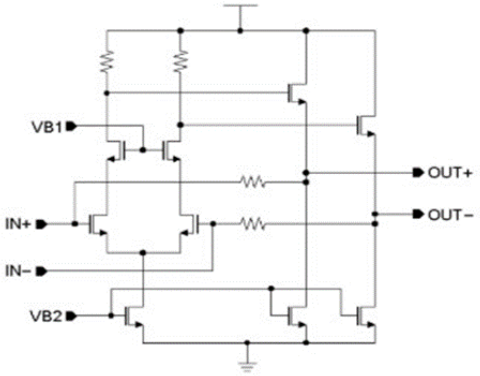

Fig. 13. Designed low noise amplifier schematic using shunt resistive feedback

[12] Power gain of 13.5dB and noise figure of 1.5 dB. The output insertion loss S22 is -9dB.input return loss (S11) is 22db.

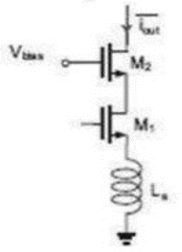

Fig. 14. Cascade LNA

[13] The NF of the circuit is 3.9 dB while the corresponding IIP3 is 4.9 dBm.

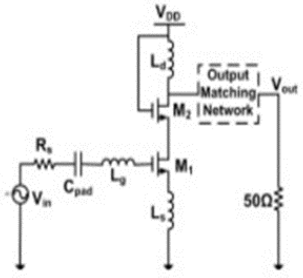

Fig. 15. Schematic representation of cascade LNA

[20] LNA achieves up to 14dB power gain with a low noise figure (NF) of 2dB and provides a reasonably acceptable input and output matching of -10dB across the frequency range of 3~5GHz.

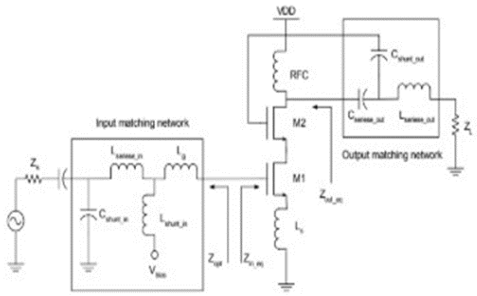

Fig. 16. Overall LNA design

[19] S11 is 14dB, S21 is 18dB with 3dB-BW of 300MHz and NF is about 1.8dB.

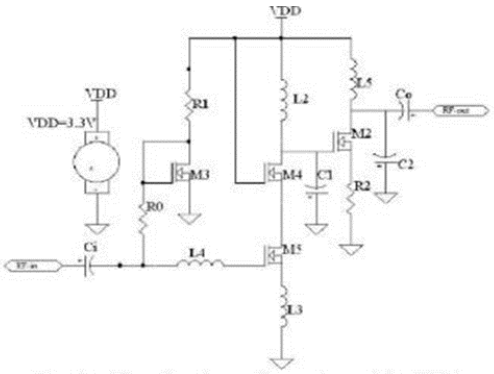

Fig. 17. The circuit configuration of the LNA

[16] 3.3V supply gives a noise figure NF of 3.5dB, a gain of 10 dB and an OIP3 of 30dBm with a supply current of 38mA.

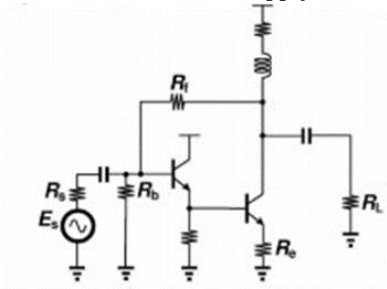

Fig. 18. LNA implementation

3. Review of outcomes using different technologies

Technology	Frequency	Gain(S21)	Noise figure	Input return loss(S11)	Output return loss(S22)	Input VSWR(VSWRin)	Output VSWR(VSWRout)
FET	6GHZ	30db	2.3db	<-10db	<-10db	-	-
Q-method (single stage LNA)	3.5GHZ	10.288db	1.062db	-	-	1.81	-
(cascode LNA)	4.5GHZ	20.317db	1.123db	-	-	1.473	-
BJT	1GHZ	3.296db	0.359db	-6.022db	1.447db	-	-
Si BJT	0.88GHZ	15.8db	1.3db	-	-	-	-
BJT	2.2-2.6GHZ	10.1db	2.01db	-	-	1.460db	1.501db
HBT(Infineon)	400-800MHZ	24-25db	<1.4db	11db	19db	-	-
SiGe HBT	410MHZ	>=20db	0.8db	-	-	-	-
BICMOS Technology	40MHZ to 1GHZ	10db	3.5db	-	-	-	-
90 nm cmos	28.9GHZ	5.9db	3.9db	-	-	-	-
130nm cmostechnology	3.5GHZ	9.6db	2.3-2.5db	<-10db	-	-	-
90nm cmos technology	60GHZ	8.06db	2.14db	-	-	-	-
Hybrid technology	10GHZ	9.110db	2.293db	-10.002db	-13.019db	-	-
0.25microM Cmos technology	2.4GHZ	21.63db	1.8db	-13.4db	-18.3db	-	-
0.18microM Cmos technology	2-10.1GHZ	10.2db	3.68db	<-9.76db	-	-	-
Cmos(SMT)	5.8GHZ	10db	-	-	-	-	-
0.25microM Cmos technology	915MHZ	12.4db	4.2db	-	-	-	-
0.18microM Cmos technology	3-5GHZ	<14db	2db	<-10db	<-10db	-	-
Sicmos	2.1GHZ	8.9/8.8db	3.14/3.1db	-17.5/-21.6d	-26.6/-31.6d	-	-

4. Conclusion

Here we observed that the reference paper [7], amplifier exhibits 3.296dB small signal gain, reverse isolation of -6.68dB and 0.359 noise figure at 1GHz. By using cascade configuration and utilizing inductive emitter degeneration, the design exhibits good input impedance, which is close to 50ohms.Which gives the best result as compared to other technologies.

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