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Design and Simulation of 1-bit Full Subtractor using Different XOR Gates

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***Abstract*: In this paper a 1 bit full subtractor is designed. In VLSI a digital circuit is designed with distinct techniques and most used techniques are CMOS technique and GDI technique. We opt a circuit which has less delay and low power consumption. In this paper a 1-bit full subtractors are designed using different XOR gates and GDI technique. The transient analysis is performed in 180nm, 130nm, 90nm, 45nm. In this analysis we found that XOR based subtractor gives less delay and GDI based subtractor gives low power consumption as compared to other circuits respectively.**

***Keywords*: 1-bit full subtractor, GDI technique, XOR gate.**

1. Introduction

A subtractor is a combinational digital circuit. Which performs subtraction among binary bits. The output is difference and borrow.

Subtractor is one of the basic arithmetic operator. In day to day life we came across many electronic components like computers, mobile phones, digital calculators, digital watches and gaming console etc., has subtractor as an important component. The subtractor is used to perform subtraction operation between 1bit, 2bits etc.

Subtractors are of two types

1. Half subtractor
2. Full subtractor

1) Half subtractor

Half subtractor is a combinational digital circuit which is used to subtract one single binary number from another single binary number. A half subtractor is one which has two inputs and two outputs.

2) Full subtractor

Full subtractor is a combinational digital circuit which is used to subtract three binary numbers. A full subtractor has three inputs and two outputs.

In this paper a 1-bit full subtractor is designed using different XOR gates using "PYXIS" design suite is a software suite produced by "MENTOR GRAPHICS" for schematic design. A six different XOR gates are designed among these five are CMOS based XOR gates and other one is GDI based XOR gate. All these XOR gates differ in their design perspective.

2. Review of XOR gates

Different XOR gate circuits are presented to implement 1-bit full subtractor. The important characteristics are to minimize glitches and power consumption.

A. XOR GATE type-1

Type-1 XOR gate is shown in below figure(a) which is designed using double pass transistor logic(DPL). This structure has 6 transistors with four inverters this leads to inverse in power consumption of the circuit. Due to inverters intermediate node have high capacitance. Hence size of transistors in not gate should increase to get lower delay. This in turn increases power consumption of the circuit.

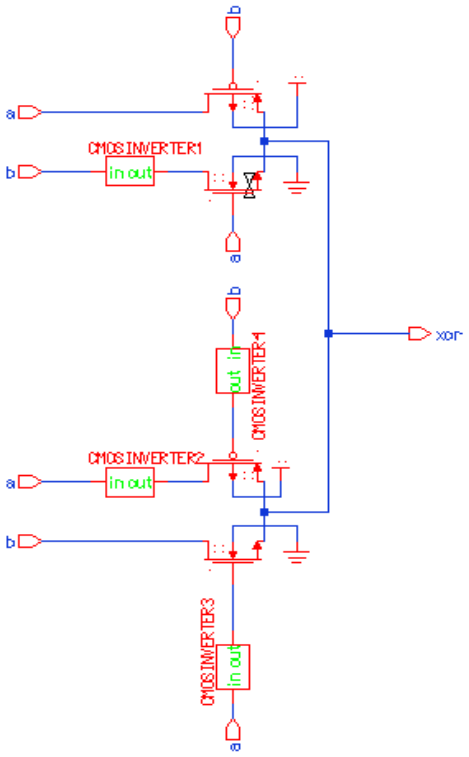

Fig. 1. Circuit diagram of XNOR gate type-1

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B. *XOR GATE type-2*

The XOR gate of type 2 is shown in below figure(b) which is designed using transmission gate and pass transistor logic. This structure has 4 number of transistors with two inverters to invert the input signal. Due to this inverter delay and power consumption are increased.

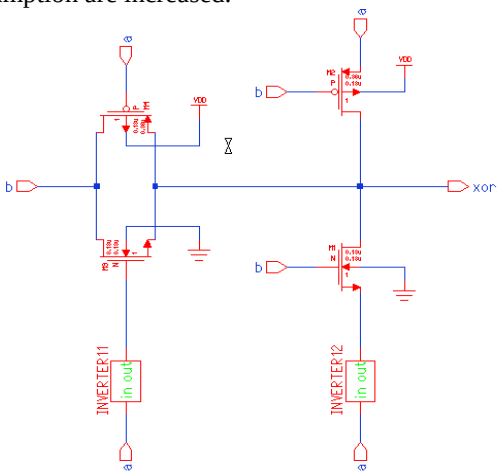

Fig. 2. Circuit diagram of XNOR gate type-2

C. *XOR GATE type-3*

Type-3 XOR gate is shown in below figure 3, which is designed using CPL and inverters. In this the output is driven by NMOS transistors and two PMOS transistors are connected to output as shown in below figure. Here delay is decreased by increasing size of the transistors.

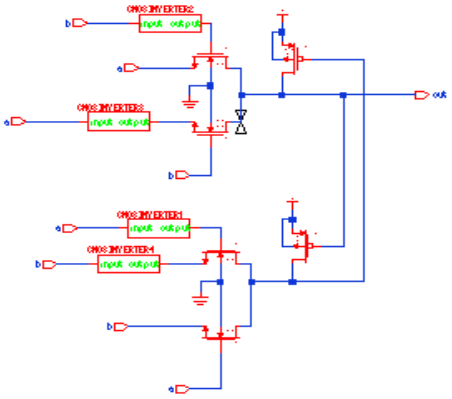

Fig. 3. Circuit diagram of XNOR gate type-3

D. *XOR GATE type-4*

Type-4 is the modified version of the type-3. This structure has 6 transistors with 2 inverters this circuit consumes less power but at the cost of delay and short circuit dominate in the circuit. Hence proper sizing is necessary. Type-4 XOR gate is shown in below figure 4.

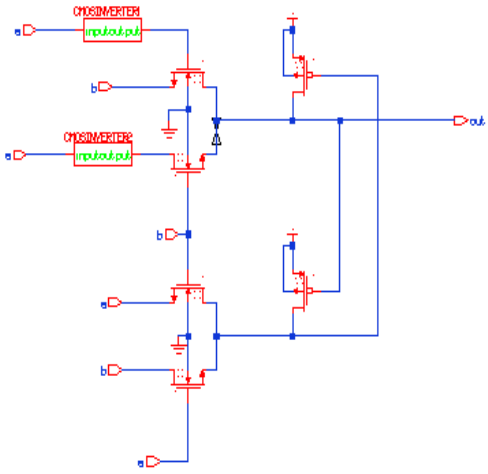

Fig. 4. Circuit diagram of XNOR gate type-4

E. *XOR GATE type-5*

Type-5 XOR gate has shown in below fig. 5, which has 4 no of transistors. The circuit is implemented with CPL and 2 inverters.

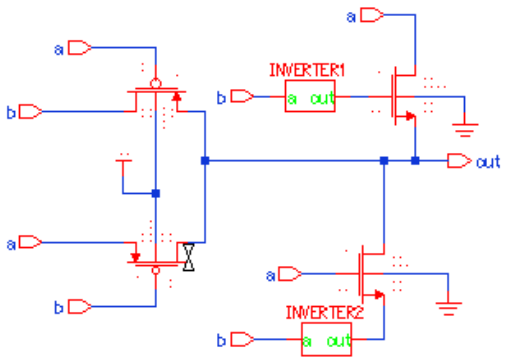

Fig. 5. Circuit diagram of XNOR gate type-5

F. *GDI based XOR GATE*

A 6t based GDI XOR gate is shown in below figure 6.

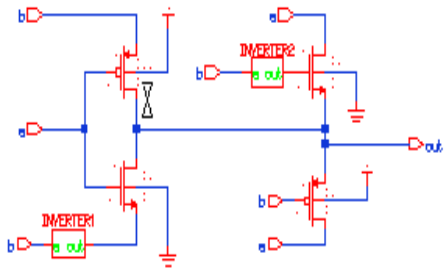

Fig. 6. Circuit diagram of GDI based XOR gate

At A=0, B=0 the NMOS transistor is switched off and PMOS

transistor is switched on, now the output is 0.

At A=0, B=1 NMOS is cut off Vin< Vth, the PMOS in the linear region Vin–Vth < Vout < VDD, then the output of XOR equal to VDD passes through PMOS.

At A=1, B=0 the PMOS transistor is switched off and NMOS transistor is switched on, where PMOS is cut off Vin<Vtp and NMOS in the linear region Vin–Vtn < Vout < VDD then the output of the XOR gate is equal to VDD-Vtn, (Vtn) threshold voltage of NMOS transistor.

At A=1, B=1 PMOS is cut off and NMOS in the linear region, then the output equal to ground passes through NMOS.

3. Implementation of full subtractor

A 1-bit full subtractor is designed using CMOS technology and GDI technology.

A CMOS subtractor is designed using CMOS based AND, OR, XOR gates.

A GDI subtractor is designed using GDI based AND, OR, XOR gates.

The schematic of 1-bit full subtractor is shown in below figure 7.

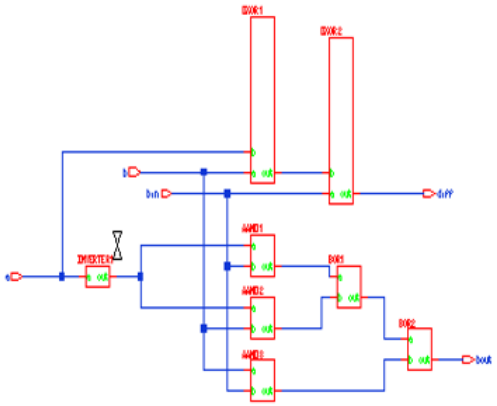

Fig. 7. Schematic of 1-bit full subtractor

4. Results

A. Simulation results of 180nm technology

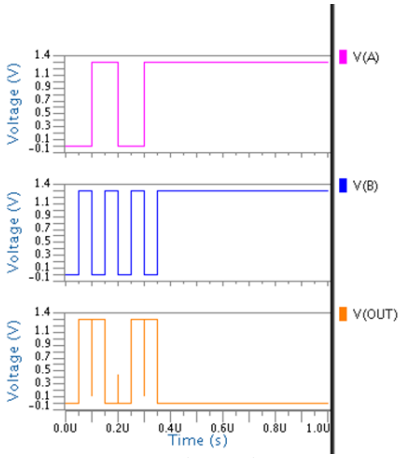

Fig. 8. Waveforms of XOR gate

A two input XOR gate gives output true when either of input is true and false when both the inputs are equal.

Table 1
Truth of XOR gate

Input A	Input B	output
0	0	0
0	1	1
1	0	1
1	1	0

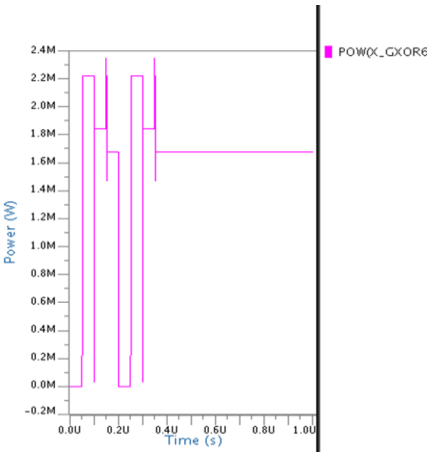

Fig. 9. Power waveform of XOR gate

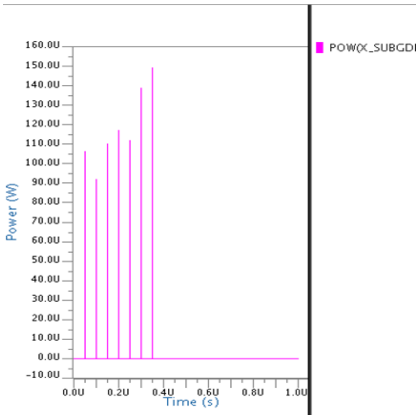

Fig. 10. Power waveform of subtractor

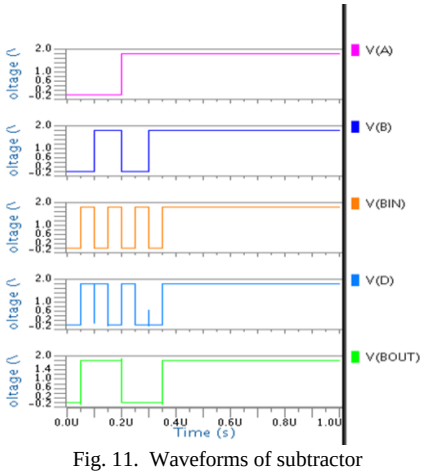

Fig. 11. Waveforms of subtractor

The table 2 shows three inputs namely A, B, bin and the two outputs are Diff, bout. Here the inputs indicate minuend, subtrahend and previous barrow.

From the subtractor circuit we can see that the two XOR gates combines to form three input XOR gate and gives output as difference of three input binary numbers.

Again from the subtractor circuit the output of three and gates is applied as an input to OR gates. Therefore, the output of OR gates is difference of three binary numbers.

Power and delay comparison of XOR gates and subtractor is show in table 3 and table 4.

Table 2
Truth of subtractor

A	B	B_{in}	Diff	b_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Table 3
Power and Delay comparison of XOR gates

Technology / XOR gate	180nm		130nm		90nm		45nm	
	Delay	Power	Delay	Power	Delay	Power	Delay	Power
XOR gate type-1	177.68ps	1.5765mw	149.72ns	211.02nw	50.204ns	594.20nw	50.197ns	1.3906uw
XOR gate type-2	193.86ps	1.626mw	50.278ns	527.41nw	49.994ns	314.76nw	49.997ns	846.96nw
XOR gate type-3	50.016ns	299.63nw	150.12ns	904.28nw	99.684ns	15.568uw	50.034ns	2.1452uw
XOR gate type-4	359.24ps	251.17uw	50.045ns	438.69nw	100.25ns	30.788uw	150.14ns	1.5374uw
XOR gate type-5	224.17ps	1.7754mw	298.18ps	281.78nw	100.04ns	3.9097mw	49.933ns	1.1011uw
GDI XOR gate	50.191ns	98.422nw	49.567ns	527.41nw	49.892ns	299.16nw	49.912ns	729.98nw

Table 4
Power and Delay comparison of Subtractor

Technology / Subtractors	180nm		130nm		90nm		45nm	
	Delay	power	Delay	power	Delay	power	Delay	power
Subtractors with XOR Gate type-1	138.33ps	517.33nw	158.4ps	4.13uw	149.95ns	13.68mw	149.93ns	14.2mw
Subtractors with XOR Gate type-2	363.84ps	353.72nw	291.73ps	1.29uw	149.96ns	14.89mw	149.96ns	15.18mw
Subtractors with XOR Gate type-3	152.69ps	772.13nw	176.04ps	1.873uw	99.944ns	87.213uw	99.906ns	143.96uw
Subtractors with XOR Gate type-4	148.76ps	607.27nw	401.84ps	1.24uw	304.71ps	120.48uw	289.14ps	186.6uw
Subtractors with XOR Gate type-5	388.25ps	415.09nw	401.84ps	1.01uw	149.97ns	9.9mw	149.99ns	10.22mw
GDI based Subtractor	380.39ps	211.75nw	212.81ps	567.94nw	149.96ns	14.89mw	149.96ns	15.18mw

5. Conclusion

In analysis, a 1-bit full subtractor can be designed using different techniques. In this paper, we performed transient analysis for XOR based and GDI based 1-bit full subtractor it is found that XOR based subtractor gives less delay when compared to GDI technique. The GDI based full subtractor gives low power consumption compared to CMOS technology. XOR based full subtractor has delay of 138.33ps and GDI based subtractor has power consumption of 211.75nw in 180nm technology. It is found that 180nm technology gives less delay and low power consumption when compared to remaining three techniques respectively.

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