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Vedic Maths Calculator using VLSI Implementation

Aakanksha Singh[1], Shivangi Tyagi[2], Harshada Ugale[3], Priti Shende[4]
[1,2,3]*UG Student, Dept. of Electronics and Telecommunication Engg., Dr. D. Y. Patil Inst. of Tech., Pune, India*
[4]*Asst. Professor, Dept. of Electronics and Telecommunication Engg., Dr. D. Y. Patil Inst. of Tech., Pune, India*

***Abstract*: Various arithmetic operations can be performed using Vedic Mathematics in less time. This paper introduces the concept of 8-bit vedic multiplier and 8-bit vedic division. Using vedic mathematic's general techniques and specific techniques, numerical calculations can be done very fast and accurately. Vedic mathematics is a technique which uses almost 16-sutras to obtain the result of various mathematic calculations. For the designing of 8x8 bit high speed multiplier the vedic mechanism used is Urdhva-triyakbhyam sutra, for the designing of 8-bit vedic divider the vedic mechanism used is Paravartya-Yojayet sutra. The working of sutra is accomplished by vertical and cross multiplication followed by successive addtion. Paravartya-Yojayet literally means transpose and apply mechanism. The sutras Used are the most efficient sutra's ,the performance is enhanced based on speed of execution ,minimum delay , low processing time so higher bit multipliers can be implemented .The designing of 8-bit vedic multiplier & divider is done using (VHDL) VLSI hardware descrptive language and simulated through Xilinx ISE Project Navigator 9.2i implemented on Spartan 6 FPGA Kit.**

***Keywords*: Parvartya-Yojayet sutra, Urdhva-triyakbhyam sutra, Vedic mathematics, Vedic multiplier, Vedic mathematics**

1. Introduction

This paper introduces the ancient method of Vedic mathematics Vedic mathematics is totally different from the conventional methods which are used to solve various arithmetic calculations it reduces the complexity of solving the mathematical problems by using simple rules and procedures it is a unique technique of calculation. Mathematics derived from Veda provides mental one line methods for super-fast calculations and cross check systems. Various operations are implemented using Vedic mathematics like multiplication, division, addition & subtraction. Vedic mathematics is based on 16 sutras. The important arithmetic operations are having wide application in different areas of engineering & technology. The performance of any circuit is evaluated by the speed of processing therefore the need for faster processing time and speed with minimum delay is becoming a major issue in the development of processor, multipliers are the key most important part of processing systems, we need to design multipliers which have either of the characteristics – high speed, low power consumption. Multipliers are used in various applications the most efficient is Urdhva-triyakbhyam sutra, which uses vertical and crosswise method. The proposed paper work also focuses on division operation based on Parvartya-yojayet which means transpose and apply mechanism. Division is an important operation in areas such as image processing, networking, signal processing, computer graphics, numerical applications, cryptography, linear productive coding for speech processing, DSP and in processor implementation. Implementing these methods of multiplication and division on digital hardware systems will be more useful for processing systems. In this paper we define the implementation of vedic mathematical methods of 8x8 bit multiplication and division in VHDL language.

A. Motivation

In Vedic mathematics, unlike the conventional methods, there are many ways to reach at a solution for a problem this gives us the liberty to choose the technique most convenient for us. The Vedic mathematics technique is more fast and accurate as compared to the conventional method of arriving at mathematical problems. The complexity of arithmetic procedures is reduced to a high level. The Vedic mathematics approach is a lot different and can be understood easily by humans of any caliber in an easy way it enriches the ability to approach and solve any mathematical problem.

2. Methodology

The objectives of this paper are, to define various Vedic maths Operations that can be implemented in VLSI, to create library for various Vedic maths operations, to implement small modules for various operations and to obtain accuracy at output using Vedic maths.

A. Multiplication

The proposed Vedic multiplier is based on the Vedic multiplication formulae (sutras). These sutras have been traditionally used for the multiplication of two numbers in the decimal number system.in this work, we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. Vedic Multiplication based on Urdhva-triyakbhyam

- "Urdhva-triyakbhyam" sutra: Urdhva-Triyakbhyam is vertically and cross wise method of multiplication which is used to find product of numbers. The idea

here is based on a concept which results in generation of all partial products along with the concurrent addition of these partial products in parallel. The parallelism in generation of partial products and their summation is demonstrated in Fig. 1.

- Using Urdhva-Triyakbhyam method. It is compatible to be used with digital hardware system. Due to its regular structure, it can be easily layout in microprocessors and designers can easily circumvent these problems to avoid catastrophic device failures.
- Methdology for 8x8 bit multiplication using Urdhva – Triyakbhyam (vertically and crosswise) for two binary numbers.

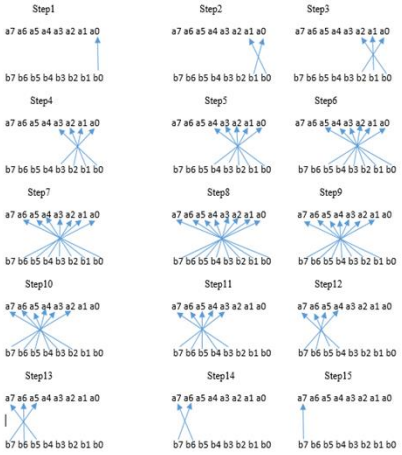

Fig. 1. 8-bit binary multiplication using Urdhva–Triyakbhyam sutra

Design of 8x8 vedic multiplier: The design of 8x8 block will be grouping the 4 bit (nibble)of each 8 bit input. These quadruple terms will form vertical and crosswise product terms. Each input bit-quadruple is handled by a separate 4x4 Vedic multiplier to produce eight partial product rows . These partial product rows are then added in an 8-bit carry look ahead adder optimally to generate final product bits. The Fig. 2 shows the schematic of an 8x8 block designed using 4x4 blocks. The partial products represent the Urdhva vertical and cross product terms. Then using or and half adder assembly to find the final product.

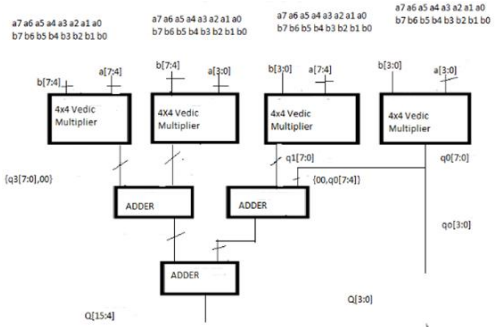

Fig. 2. Block diagram of 8x8 multiplier

B. Division

In this paper the implementation of a low power and high speed Vedic divider based on ancient Indian Vedic Mathematics. Using "Parvartya-Yojayet" sutra the propagation delay and power consumption are reduced to an extent. Divider is basic Hardware employs in high speed and advanced digital signal processing. The sutra's used in Vedic mathematics reduce the iterations for complex circuitry

"Parvartya-Yojayet" sutra: - Division algorithm for decimal numbers is implemented based on" Parvartya-Yojayet-Transpose and apply". Division has important role in high precision radar technology, cryptography, in cloud data storage, speech processing because of which Parvartya-Yojayet sutra is used for faster processing.

Methodology for Vedic division using PY sutra:

Table 1
Vedic algorithm for 8 by 4-bit division

Divisor	Dividend
0 1 1 0	1 0 1 1 0 0 0 0
-0 -0 1	-0 -0 1
	0 0 0
	-0 -0 1
	0 0 0
	-0 -0 1

Table 2
Quotient & Remainder for 8 by 4-bit division

	1 0 -1 0 1	1 0 1
	Q=10001-110	R=101
	Q=10111	

Hardware realization for 8 by 4-bit division: The Vedic divider block consists of A0A1A2A3A4A5A6A7 as dividend digits and B1B2B3 as divisor digits. At first A0 is partially multiplied with complemented divisor digits B1, B2 and B3. Multiplied data added with dividend input A1 and then again summation results are multiplied with complemented divisor digits. Each successive addition result is used as one of the multiplicand for further partial multiplication. This cycle repeats until addition results for A7 are carried out. During addition carries generate from one row propagates to next row as per sutra.

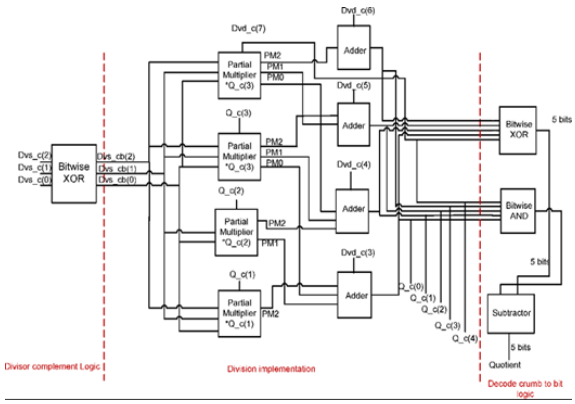

Fig. 3. Block diagram of 8 by 4-bit Vedic divider

3. Result and analysis

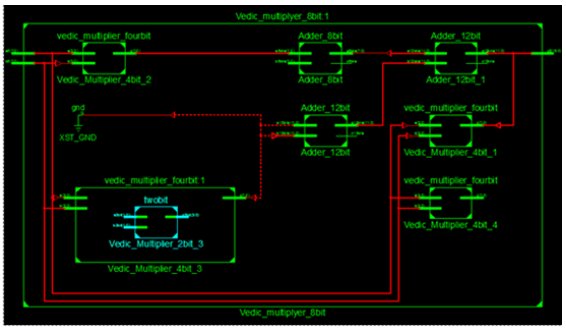

Fig. 4. RTL Schematic of 8x8 Vedic multiplier

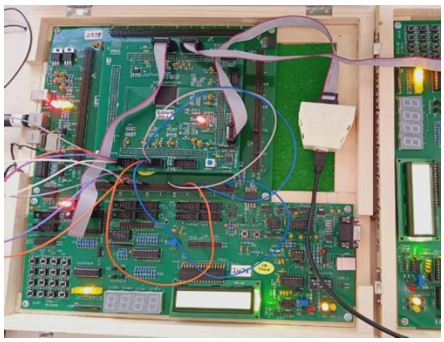

Fig. 5. Result of 8x8 Vedic multiplier on Spartan-6 FPGA kit

4. Conclusion

From this paper we conclude that a high speed, low power 8x8 vedic multiplier can be implemented using Urdhva Triyakbhyam Sutra. The proposed vedic divider is implemented using binary format using Parvartya-Yojayet sutra.

References

[1] Urga Mohan Kumar, Sandeep Kumar, Madan Pal Singh, Ashok Kumar Yadav, "Fast and Efficient Division Technique Using Vedic Mathematics in Verilog Code," International Journal of Scientific & Engineering Research, vol. 8, Issue 10, October 2017.

[2] Deepak Kumar, Prabir Saha and Anup Dandapat, "Vedic algorithm for cubic computation and VLSI implementation," Engineering Science and Technology, an International Journal paper, (2017), 1494-1499.

[3] Jyoti Kumawat, and Sunil Sharma, "A 8x8 bit multiplier using Vedic Mathematics," International Journal of Engineering and Technical Research (IJERT, vol. 2, issue-3, March 2014.

[4] Kuldeep Singh Sidhu, and Ashwini Kumar Singla, "A low Power 16 Bit Divider for High Speed VLSI Applications," An International Journal of engineering Science, vol. 17, January 2016.