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Memory Modules - Trends in CMOS Image Sensor Technology and Design of DRAM

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***Abstract*: This paper presents the many-core architecture, with hundreds to thousands of small cores, to deliver unprecedented compute performance in an affordable power envelope. We discuss fine grain power management, memory bandwidth, on die networks, and system resiliency for the many-core system. The problem of devising a more effective information retrieval interface grows more important. Future designs may draw upon cognitive theories of categorization and metaphor to understand how users interact with text-both paper and electronics. This scheme avoids logging, but still provides the same journaling effect by simply altering the state of the cached block to frozen. As a frozen block still performs the function of caching, we show that in-place commit does not degrade cache performance. We implement our scheme on Linux 2.6.38 and measure the throughput and execution time of the scheme with various file I/O benchmarks.**

***Keywords*: Automata, Optimization, and computer screens**

1. Introduction

FLEXIBLE non-volatile memories are essential for realizing flexible electronics, including paper-like displays and radio frequency identified tags. Inorganic ferroelectric materials are used in non-volatile ferroelectric memories because of their low power consumption and high-speed writing/erasing. Both Nano magnetics and spintronics utilize spin or magnetism to provide new ways to store and process information; Nano magnetics is based mainly on magnetic interactions between Nano magnets, while spintronics is primarily associated with the utilization of spin polarized currents in memory and logic devices. With the end of complementary metal–oxide–semiconductor (CMOS) in sight, Nano magnetics can provide a new paradigm for information process using the principles of magnetic quant- tum cellular automata. FD SOI intrinsic characteristics are interesting in circuit performance optimization. Meanwhile approximate storage with spintronic devices shows promise for improvement in energy-delay trade- off and robustness. For example, NV multi-bit adder can be designed with Accurate circuit for more significant bits, whereas inexact (approximate) for less significant bits. It allows both reading and writing operation to be performed at varying quality-energy according to Design specification. A number of memory technologies are emerging as viable alternatives that address one or more of these shortcomings of DRAM. Volatile memories are one such technology, which have retention times comparable to DRAM (order of nanosecond) and also need frequent refresh, similarly to DRAM. They are based on DRAM cell technology but improve on the architecture and the interface to deliver higher performance and energy efficiency than DRAM. Moore's Law continues integration capacity to realize complex architectures, and reducing energy consumed per logic operation to keep power dissipation. Advances in software technology, such as rich multimedia applications and run time systems, exploited this performance explosion, delivering end users with higher productivity, seamless internet connectivity, and even multimedia & entertainment. It is characterized by non-volatile, small size, shock resistance, and low power consumption. The deployment of flash memory is spreading out ranging from consumer electronic devices to general purpose computer architecture. In non-volatile memories, NOR flash memory provides a fast random access speed, but it has high cost and low density compared with NAND flash memory.

2. Literature survey

The most computer systems use primarily name-oriented approaches in their depiction and display of files. Text files are best depicted on computer screens. While storing and retrieving paper documents efficiently has always been a challenge.[1] The growth of electronic text files has made the situation increasingly more problematic. The strongest evidence for this view comes from language behavior. The design of information systems and interfaces are best based on studies of user characteristics. The major problems facing system designers lies in providing methods for naming, organizing and indexing.[2] They have demonstrated that physical analogies do less well than simple naming, the experimental tasks. Most effective are those that correspond most closely to the physical environment in which we deal with documents [3]. NAND ash memory has advantages of a large storage capacity [4]. The capacity of a NAND ash memory chip became gigabyte stage, and the size will be increased quickly. Many operations are hampered by its physical characteristics. The most important feature is that bits can only be cleared by removed or eliminated. Large block of ash memory [5]. The erase operation makes dead pages become available again. It erases data between the journal region and its home location for system consistency. The redundant data copy by remapping the logical journal data location to real present location. Our JFTL can

prevent from degrading write performance of file system while preserving file system consistency [6]. Our long-term vision is the Organizational Memory (OM) at the core of a learning organization, supporting and sharing. The implementation and use specific task models is they are highly dependent on the particular applications. Modifications in the tasks which the OM shall support have to be reflected [7]. The OM shall be continuously tuned in order to better match user's needs. Adaptations. The insertion of new knowledge elements into the object level of the OM requires corresponding up dates in the knowledge description level. A vast amount of well-structured but non-formal technical documentation together with a concise domain ontology. Important goal of Artificial Intelligence has been to build knowledge-based systems. Even though the benefits of having an OM are generally recognized, organizations are reluctant to invest time and money [8]. In industrial practice, costly errors are often repeated due to an insufficient flow of information. For the same reasons as up-front knowledge engineering, maintenance efforts for an OM have to be less [9]. CMOS image sensors benefit from technology scaling by reducing pixel size, increasing resolution, and integrating. The use of shallow junction and high doping result in low photo responsively, and the use of shallow trench isolation. They have less performance than CCDs and as result are not used in digital cameras& other operations [10]. The applicability of CMOS image sensors, and to enhance their performance and dark current due to reset transistor off-current and the follower transistor gate leakage current [11]. To reduce transistor leakage. Hydrogen annealing was also shown to reduce leakage by passivation defects. Different Si ON materials are being tried out to increase light transmission. The thresholds of these two transistors are also adjusted to further reduce leakage and increase voltage swing [12]. The shape memory effect is related to the local cooperative reordering of lattice atoms. The secondary shape is obtained by deforming the material at a temperature above the soft phase [13]. The soft phase modulus increases by orders of magnitude, effectively retarding this recovery. These include implant devices, catheters, micro actuators, and optical heating of shape memory devices. The optical properties of SMP, methods for coupling laser light into SMP.[14]The thermally activated material in a blood vessel (with and without flow) are presented. The only approved therapy for treatment of acute ischemic stroke is intravenous recombinant tissue plasminogen activator. The efficacy of PA limits the window of opportunity for revascularization to three hours of symptom on set. The issue becomes the duration of the time window during which the patient would benefit.[15]Moore's Law continues with technology scaling, improving transistor performance to increase frequency. Higher the transistor integration capacity to realize complex architectures, and also reducing energy consumed per logic operation. The technology treadmill will continue, providing integration capacity of billions of transistors.[16]The evolutionary approach is to continue today's trend with a few large processor cores. Performance increase is roughly directly proportional to square root of increase in complexity. A many-core system will deliver higher compute throughput than a multi-core system.[17] Excessive sub-threshold leakage current, and supply voltage scaling slowing down. The serial percentage in a program is large, then parallel speedup saturates with small number of cores. [18] The spin of a single electron subject to a static magnetic field provides a natural two-level system that is used for use as a quantum bit. The fundamental logical unit in a quantum computer. Semiconductor quantum dots fabricated by strain driven self-assembly. They can be controllably positioned.[19] Electronically coupled and embedded into active devices. The stored electron distribution is optically probed by forward biasing the Schottky junction. [20] The lack of any circular polarization excludes the possibility that spin alignment due to inter Zeeman level thermalization occurs over such short storage times [21]. The memory element is essentially a resistor of a thin-film chalcogenide material. A low-field resistance that changes by orders of magnitudes, depending on the phase state of the material in the active region.[22] Programming requires instead a relatively large current. The name chalcogenide material and lead to a thermally induced local phase change. Future replacement of standard floating-gate based Flash cells, the phase-change memory. The feasibility assessment of large PC Mar rays has been focused on the integration with the CMOS technology. [23] The reduction of the power consumption and the scaling perspectives, while the reliability and the disturb characteristics have been only marginally addressed. The mechanisms responsible for the potential data loss and degradation will be discussed, as well as the perspective to improve the actual device performance. [24]. The prime requirement of a memory dominated embedded systems is Low energy consumption. Lowering supply voltage is one of the options to reduce the rate of power consumption.[25] Due to reduced static noise margin (SNM) and increased variability in design and process parameters. Reduce the leakage power. The density requirement is mainly limited due poor driving capacity of the bit-lines. This motivates us to explore alternative SRAM cell structure suitable for Nano scale CMOS circuits. Operating at sub threshold targeted ultra-low power applications.[26] The new approach attractive for Nano scale technology regime in which process variations is a major design constraint. The random dopant fluctuations and line edge roughness causes mismatch in design and process parameters of a device, particularly threshold voltage. The parametric failures such as read, write and access failures in SRAM can be characterized by the target value of the performance parameters such as read and hold SNM and WTP which determines the yield.[27]All electrical simulations have been performed with the Infineon internal SPICE- like simulator. Resistive opens generally cause timing-dependent faults. The occurrence of resistive-open defects has considerably increased in recent technologies. The

presence of many interconnection layers and an ever growing number of connections between each layer.[28] The most common root cause of test escapes in deep submicron technologies. Resistive defects have been injected in the Infineon 0.13µm synchronous embedded-SRAM family Due to the internal self-timed architecture, two types of timing-dependent faults can be identified.[29] The primary targets have been the study of the consequences of resistive-open defect injection because this kind of defects. The identified fault models we have focused the attention on those that have a dynamic behavior. The simulations have been performed for different values of temperature, supply voltage and process corner.[30]The reliability of memory systems that are exposed to soft errors. The aim of deriving the Mean Time to Failure (MTTF) and the probability of failing in a given time interval. The soft errors were considered to arrive following a Poisoning basis. They were assumed to be single uncorrelated events (each event causes only one soft error).[31] Multiple Bit Upsets (MBUs) are a significant part of the error events in advanced memory technologies. They will continue to grow in the next technology nodes. The errors in an MBU are normally caused by the same physical event.[32] The MTTF of a memory exposed to MBUs has been derived; and second, some approximations have been presented. Evaluating the proposed approximations on real memories is the natural extension. The experiments should first characterize the p(n) for the memory under test and the physical event causing the upsets, then compute the theoretical approximations. [33] Non-volatile memory, such as core memory, was once the choice of main memory of computers. More compact and fast thin magnetic-film memories, developed subsequently that were supposed to be non-volatile. Magnetic tunnel junctions (MTJs) are reported with their potential impacts on integrated circuits. The boundary of regions having different magnetization directions to reduce the magneto static energy, which resulted in loss of information.[34] The individual magnetic element can also be made virtually non-volatile; the cutting-edge hard-disk-drive (HDD) technology. [35] The device MRAM development trend with the International Road map for Semiconductors(ITRS) product technology trends for DRAM and Flash for comparison. We can define small magnetic elements by lithography, small enough that introduction of domain walls is energetically unfavourable. The individual magnetic element can also be made virtually non-volatile; the cutting-edge hard-disk-drive (HDD) technology has proven that magnetic grains. The high TMR ratio enabled by the MgO-barrier MTJs, together with the demonstration of CIMS at a low

Jock, allows development of not only scalable magneto resistive random-access.[36] Impacts on how other types of communicative technologies are used – such as the phone and email.[37] Online communication technologies are detrimental to off-line communication practices. We found that patterns of migration from SNS My Space to Facebook were common with one of the central reasons given was that more friends had adopted. We began our focus groups by asking participants to tell us about the people they come into contact with day to day – and try to put on a metro that relation. We found the results revealing.[38] The exercise was intended to encourage our participants to think about all the types of people during the course of their lives, and think about the terms for these respective connections. The vast majority of our participants' contact lists are not contacted at all. It will mean as one journeys through life these associations can be captured and up-to-date information about our former relationships is ready to be recalled and revived along the way. Strong desire to maintain, organize and trail associations illustrated by the mass popularity of SNS and these technologies that offer these capabilities.[39]Main memory is becoming a dominant portion of the total system energy due to the trend in increasing the memory capacity. The growing memory requirement of new applications, and the increasing number of processing cores in a single chip. The main memory can dissipate as much leakage energy as dynamic energy.[40]NAND flash also requires a block to be erased before writing into that block, which introduces considerably extra delay and energy. Probably the two most promising candidates for next generation memory technology for both standalone and embedded applications. Moreover, phase change material has excellent scalability within current CMOS fabrication methodology.[41] The memory access latency, and help improve the memory bandwidth provision in CMPs. substantial amount of dynamic energy in main memory, when compared with traditional 3D stacked DRAM. The greatest reductions come from 1) the write energy because the majority of the bit-writes are removed.[42].The proposed design strategies in this work.A thorough exploration of variability and reliability-aware ultra-low power design was performed in NV-logic gates, adders and flip-flop with respect to Vdd scaling.[43]The sensing/read mode, the power-delay efficiency of each circuit has been simulated by adjusting design factors Vdd, VBB and PB. Sensing circuit performance including circuit latency, dynamic power, leakage power, variability and sensing probability have been optimized for user-define multipurpose.[44]Leakage dominant applications, balanced leakage-dynamic applications. The power penalties with speed trade off[45].The current DDR3 power performance level of approximately 600 MW/GB/s, in an Exa scale system, the memory alone would draw 600MW.Advancements in memory technology are sought in all the significant metrics of performance, power/energy efficiency, density, and scaling. A number of memory technologies are emerging as viable alternatives that address one or more of these shortcomings.[46]DRAM Volatile memories are one such technology, which have retention times comparable to DRAM and also need frequent refresh, similarly to DRAM.A significant body of research has explored the use of NVM technologies as storage and as an alternative to DRAM. Opportunities for complementing DRAM to improve the overall performance and energy efficiency of the memory

system [47]. The impact of these technologies on High Performance Computing (HPC) and data intensive applications. Simple hierarchy of NVM following DRAM can provide energy saving of as much as 21%, with an overhead of 7% in runtime. DRAM and denser NVM form a partitioned address space.the potential of integrating emerging memory technologies in the memory hierarchy. We have not factored in the cost. [48]. High-performance computing SSDs offer substantial performance improvements relative to disk, but cost is limiting adoption. The hope of SSD manufactures is that improvements in flash density through silicon feature size scaling. We use this analysis to predict the performance and cost characteristics of future SSDs. [49]We show that future gains in density will come at significant drops in performance and reliability. SSD manufacturers and users will face a tough choice in trading off between cost, performance, capacity and reliability. Trends to make projections about the performance and cost of future SSDs. [50]The reduction in performance that is necessary to increase capacity while keeping costs in check may make it difficult for SSDs to scale as a viable technology for some applications [51].

3. Conclusion

First we presented several modifications that have been shown to enhance deep submicron CMOS technology imaging performance. We showed that such modified processes will enable (i) multi-mega pixel sensors, (ii) camera-onchip integration, (iii) per-pixel ADC, (iv) integration of embedded DRAM and processing with a sensor and (iv) wavelength selectivity via metal patterns. Finally, we discussed high frame rate applications to still and video rate imaging, in particular, dynamic range extension via multiple capture. These trends, we believe, will ultimately enhance CMOS image sensor performance beyond that of CCDs. In addition to high speed imaging applications, several researchers have recently shown that high frame rate can also benefit still and video rate imaging. The idea is to use the high frame rate to oversample the scene thus obtaining more accurate information about illumination and motion. This information can then be used to: (i) enhance image quality, (ii) improve the performance of video applications, or (iii) simplify many low-level vision algorithms, e.g., feature tracking.

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