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Study and Implementation of RAM Cell using a Novel 5 Input Majority Gate in QCA

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***Abstract*: QCA (Quantum-dot Cellular Automata) may be a promising new technology with low power consumption and high speed that permits the planning of Nano scale integrated circuits. The three- input and one-output majority gate is that the basic building block in QCA circuits. This work presents a replacement style of a multi-output, 5- input majority gate. Our projected gate is sort of helpful as a result of its outputs will gift totally different configurations with many logical functions right away, facultative the planning of smaller circuits. Also, the projected gate may be a possible resolution for the recently projected USE (Universal, Scalar and Efficient) duration theme. so as to demonstrate the pliability and space potency of our 5-input majority gates we tend to implement 2 designs: a full adder and a RAM cell block. These styles are enforced employing a free and a daily (USE) clock schemes. Our results show space reductions compared to the prevailing one.**

***Keywords*: QCA, RAM cell**

1. Introduction

Number of transistors in CMOS technology follows Moor's law. For coming up with digital circuits during this technology, binary info is coded within the style of current switches. Within the different word, once the switch is on that suggests that binary "1" and once the switch is off it suggests that binary "0". to realize a circuit with higher speed and lower power consumption, size of semiconductor unit ought to be cut. However, as this technology moves below sub-micron levels several issues arise. Some physical limitations like quantum result, unpredictable behaviour in low currents and a few limitations that or associated with this technology like power consumption, style and lithography quality stop developing micro-electronic systems that follow Moor's law. thus there's a requirement to a brand new technology to code the binary info. For developing new and sensible technologies for coming up with Nano-scale circuits, some new solutions ought to be thought-about. within the recent years several researches are investigated so as to style Nano-scale circuits victimisation Quantum Cellular Automata (QCA) technology and scientists and designers of the digital circuit hope that CMOS are going to be replaced with this novel technology. Basic operation and performance of a QCA cell are proven and physically enforced. These styles embrace not solely little styles like associate degree Adder or XOR however conjointly massive styles like a processor.

A. QCA introduction

QCA may be a novel rising technology within which logic states don't seem to be hold on as voltage levels, however rather the position of individual electrons. Conceptually, QCA represents binary data by utilizing a bi stable charge configuration instead of a current switch. not like standard logic circuits within which data is transferred by electrical current, QCA operates by the Columbic interaction that connects the state of 1 cell to the state of its neighbours. thus {the data the knowledge the data} transfer (interconnection) is that the same as information transformation (logic manipulation) within the QCA technology.

During this chapter you may find out about a promising future engineering for computing. It takes nice advantage of a physical effect: The Coulomb force that interacts between electrons. There additionally exists an alternate implementation that uses magnetic fields, however this sensible course won't cowl magnetic QCA for currently. although it's still troublesome to supply and operate with these devices below typical temperature conditions, simulations predict promising numbers, like theoretical clock rates of many terahertzes. The QCA cell in distinction to physical science supported transistors, QCA doesn't operate by the transport of electrons, however by the adjustment of electrons in an exceedingly little restricted space of solely many sq. nano meters. QCA is enforced by quadratic cells, the alleged QCA cells. In these squares, specifically four potential wells square measure situated, one in every corner of the QCA cell (see figure 1). within the QCA cells, specifically 2 electrons square measure fastened in. they will solely reside within the potential wells. The potential wells square measure connected with lepton tunnel junctions. There square measure 2 diagonals in an exceedingly sq., which implies the electrons will reside in just 2 potential changes within the QCA cell. relating to these 2 arrangements, they're understood as a binary '0' and binary '1', i.e. every cell may be in 2 states. The state '0' and therefore the state '1', as shown in figure three. A binary number system are some things acquainted, as symbolic logic is employed already in today's computers. There, a high voltage is commonly understood as binary '1' and an occasional voltage as binary '0'.

B. *Existing method*

Recently, a replacement continuance theme, particularly USE (Universal, climbable and efficient), has been planned for clock distribution in QCA circuits. It solves one in all the foremost limiting factors of existing clock schemes, the implementation of feedback methods, that facilitates QCA circuit routing, and additionally avoids natural philosophy issues. With this clock theme one will specialize in the look of the circuit and ignore those issues. Also, a typical cell library has been designed supported USE clock theme. The 3 primitives in QCA or the 3-input majority gate, electrical converter and wire. within the existing system, three input and one output majority gate is employed, that isn't appropriate for the employment continuance schemes.

C. *Proposed method*

In the projected technique we propose a replacement style of a multi-output, 5- input majority gate. Our projected gate is kind of helpful as a result of its outputs will gift totally different configurations with many logical functions directly, enabling the look of smaller circuits. Also, the projected gate could be a possible resolution for the recently projected USE (Universal, Scalar and Efficient) continuance theme. during this work we have a tendency to gift a multi-output, 5-input majority gate that takes into account the restrictions that USE theme brings to the data flow of a QCA circuit. we have a tendency to use the projected gate to implement 2 circuits, a full adder and a RAM cell.

2. Basic of majority gate

A. *Clock zones*

Clock zones are a difficult challenge of QCA. They avoid random changes of QCA cells and "guide" the data flow, especially the information propagation, through QCA circuits. In distinction to transistor-based circuits, one clock cycle consists of 4 clock signals, that or delayed by ¼ of the entire clock cycle among one another, as portrayed in figure eleven.

The figures during this chapter can perpetually show clock zones like clock zero, clock one and then on. this is often for convenience; in fact, you'll additionally browse it as clock n, clock n+1, clock n+2. necessary is, that exact teams of QCA cells square measure in several clock zones. once the clock signal is high, it opens the lepton tunnel junctions in QCA cells. Opened tunnel junctions enable the 2 electrons during a QCA cell to travel between potential wells. reckoning on the encompassing Coulomb forces round the QCA cell, the electrons can travel various potential wells.

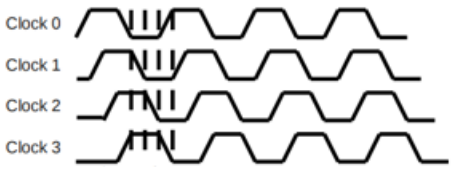


Fig. 1. The four shifted clock signals

There is a rough higher limit for the dimensions of 1 clock zone. In QCA wires with nearly no alternative QCA cells close to the wire, i.e. with no Coulomb force "noise" from the encompassing, clock zones may be giant. In areas with QCA cells round the wire, the clock zones should be smaller. there's no strict rule for the dimensions of a clock zone keen about the encompassing noise, however generally it seems that in clamorous areas clock zones might need to be as tiny as solely 2 QCA cells.

In areas with nearly no noise, clock zones may be designed as giant as 12-14 QCA cells. there aren't any strict rules wherever to start and finish a clock zone, there's some best observe, a way to place clock zones round the basic gates, conferred within the previous chapters. after you style QCA circuits, we have a tendency to powerfully advocate to stay to those clock zones, there exist solely terribly rare cases wherever clock zones round the basic gates will take issue while not poignant reliable information propagation.

3. Input gates

A. *Basic element and gates*

So far, we all know the way to interpret and transport info with QCA cells, however nevertheless we have a tendency to lack the chance for computations. For QCA cells the fundamental gate may be a three-input majority vote. it's engineered from 5 cells, organized as a cross.

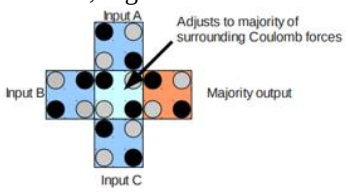


Fig. 2. QCA majority voter

B. *QCA majority voter*

From physics, it's understand that the Coulomb forces of many electrons add up. the bulk elector takes advantage of this result. The cells on prime, at the left and at very cheap work as input association cells. because the Coulomb forces of the electrons of all input cells add up, the center cell adjusts to the bulk of changes of the input association cells. Finally, the output cell adjusts to the center cell and also the ensuing state of the bulk vote will be obtained from the output cell. 4.2 QCA gate as we have a tendency to add the sector of QCA with the legendary binary illustration, it's desirable to own any logic gates we have a tendency to already accustomed to. By a small modification, it's doable to show the bulk elector into associate degree gate.

The mathematician AND outputs one if all inputs or one, otherwise zero. relating to 2 inputs of the bulk vote, because the inputs of associate degree gate, and also the elector shouldn't output one if only 1 of the 2 inputs is one, a hard and fast cell is intercalary as third input, that forever is within the zero state. If each AND inputs are one, the 2 1s add up to a stronger Coulomb

force than the only mounted zero cell and also the majority elector is become a two-input gate (see figure 3). The mounted cell will be obtained by setting it to the zero state and ne'er open the tunnel junctions.

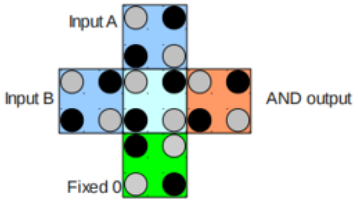


Fig. 3. QCA AND gate

C. QCA OR gate

The logic gate is constructed virtually precisely just like the AND circuit, however rather than a set zero, a set one QCA cell should be hooked up united input. The mounted one cell sums up to a stronger Coulomb force with one different input being adjusted to one, so the logic gate can output one.

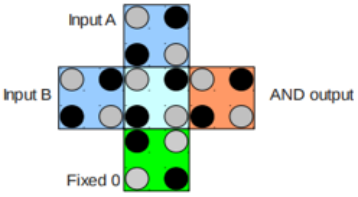
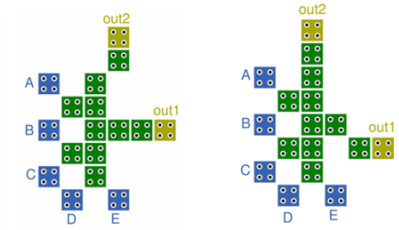


Fig. 4. QCA OR gate

D. Five input gates



(b) Configuration 2: *out1* = Minority *out2* = Majority

(c) Configuration 3: *out1* = Majority *out2* = Minority

Fig. 5. Five input gates

Our M AJ5 will assume four configurations with 2 outputs that may be set each as Majority or Minority gates, increasing our M AJ5 gate flexibility. we will perform the output configuration as majority or minority by moving the last cell before the various output. we will observe all doable configurations in Fig.2, wherever blue and yellow cells represent the inputs, and therefore the outputs, severally. This multi-output theme is beneficial to facilitate circuit routing and cut back the number of gates since each Majority and Minority operations will be enforced in any given gate.

In addition to having 2 doable outputs, another important advantage of the planned M AJ5 is that a similar style will be accustomed implement many completely different logic function.

4. Circuit design

A. Full adder using M AJ5

Our adder uses 2 MAJ5 gates to modify the planning layout. ancient styles use 3 3-input majority gates (MAJ3), wires, and inverters. Moreover, our style takes advantage of the MAJ5 ability to implement a multiple-output MAJ3, by fixing the values of inputs D and E in +1 and -1, severally. we'd like 2 results from one gate at an equivalent time, one could be a 3-input majority operate to calculate the carry and the opposite could be a 3-input minority as inputs to calculate the total. the complete adder is shown in Fig. 6.

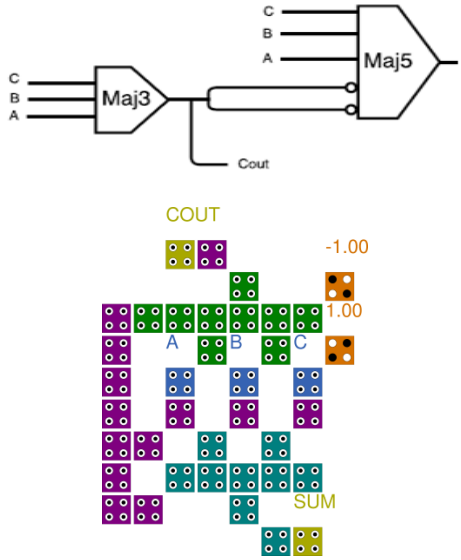


Fig. 6. Full adder

B. RAM cell

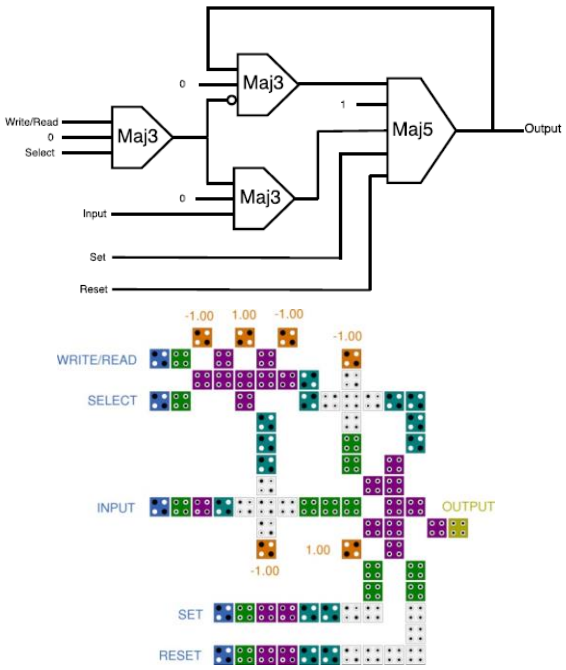


Fig. 7. RAM cell

Another attention-grabbing circuit that takes advantage of our planned MAJ5 is that the RAM memory cell reveals the schematic of the circuit, having 3 MAJ3 and one MAJ5 gates. The left MAJ3 implements AN gate and its outputs area unit connected as inputs within the alternative 2 MAJ3. The latter area unit easy 2-input AND gates with one output. Finally, they hook up with a MAJ5.The leftmostMAJ3 is enforced by a MAJ5 so as to take advantage of its multiple outputs options.

C. Result

Here we tend to compare our full adder and therefore the RAM memory

cell with different implementations obtainable in literature. All circuits proposed during this work are simulated victimisation QCA De- signer through the coherence vector simulation engine. The comparison between our projected full adder and people enforced in different works. the primary column shows the look, second column presents the circuit size in terms of range of QCA cells, and third column shows the delay in terms of QCA duration zones. Finally, the last column details if the look uses multilayer. The first 5 styles are enforced victimisation the free clock theme. we will see that our adder outperforms 3 of them, considering the quantity of cells. The delay is nearly constant all told circuits. the primary four circuits apply 5-input majority gates. Our circuit has constant size and delay than the look projected. Despite the latter solely apply 3-input majority gate, they use multilayer approach to implement a compact circuit. However, multilayer may be big-ticket and troublesome to be enforced. So, it's a decent strategy to reduce it. Our adder, on the opposite hand, presents a flattened style.

5. Conclusion

In this work, we have a tendency to planned a completely unique 5-input, multi-output majority gate for QCA technology. Our gate has many features such as: 2 outputs which will be organized as each majority and minority; ability to perform completely different logic functions by simple fixing a number of the inputs; economical layout in free and USE clock schemes. we have a tendency to used our gate to implement a full adder and a RAM memory cell styles. For each styles we have enforced free and USE clock schemes. Our results support our claims of the potency and adaptability of our gate. We not solely reduced the styles areas however conjointly the delay.

References

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