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# Design of Low Power Comparator for 10-bit SAR ADC in Biomedical Applications

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***Abstract*: power consumption is one of the main design constraints in today ICs. For system that ae powered by small non rechargeable batteries over the entire life time, such as medical implant devices ultralow power consumptions is important. In these systems ADCs are key components to interface between analog world and digital domain. The comparator in the SAR ADC takes more power consumption than other blocks. Additionally, it focuses on selection of suitable dynamic comparator architecture. Based on this analysis, dynamic two-stage comparator is selected due to its energy efficiency and capability of working in low supply voltages .Eventually, based on these studies an ultra-low power 10-bit SAR ADC in 65 nm technology is designed. Simulation results predict that the ADC consumes 12.4nW and achieves an energy efficiency of 14.7fJ/conversion at supply voltage of 1V and sampling frequency of 1KS/s. It has a single-to-noise-and-distortion (SINAD) ratio of 60.29dB and effective-number-of- bits (ENOB) of 9.72 bits. The ADC is functional down to supply voltage of 0.5V with proper performance and minimal power consumption of 6.28nW.**

***Keywords*: Low Power, SAR ADC, SAR LOGIC, dynamic Comparator,**

## 1. Introduction

Analog to digital converters are important building blocks in lots of Applications. In past few years, more and more applications are built with very stringent requirements on power consumption. For electronic system such as wireless system or implantable devices, the power consumption is becoming one of the most critical factors. The stringent requirements on the energy consumption increase the need for the development of low voltage and low power circuit techniques and system building blocks.

Analog to Digital converters translate the analog quantities into digital language, used in information processing, computing , data transmission and control systems. ADC SAR key components for the design power limited systems,in order to keep the power consumption as low as possible. Implantable medical electronics, such as Face Makers and Cardiac Defibrillators are typical examples of devices where ultra low power consumption is paramount the implanted units relay on a small non rechargeable battery sustain a lifespan of Up to 10 years. The life time of the artificial pacemakers should last upto 10 years which mandate low power consumption for operation. The analog to digital converters is the crucial part of an implanteable pacemakers since it consumes a large amount of power as the interface between sensed analog signal and digital signal processor block. Low power ADCs with moderate resolution and low sampling frequency is suited for biomedical applications.These specifications make SAR ADC the suitable choice it consumes low power due to its simple structure. Moreover, SAR ADC is scalable with the technology scaling since most parts of the architecture apart from the comparator are digital. The rest of the paper is organized as follows; one biomedical device pacemaker operation is explained in section. SAR ADC architecture operation is explained in below section.

## 2. Pacemaker operation

Pacemakers directly control the pattern and speed of the heartbeat. When the heart stops beating are it beats slowly, pacemaker provides weak electrical signal with approximately 70 beats per minute to correct the timing of heartbeat. This medical device contains a battery, a generator and pacing leads. The leads connect the pacemaker to the heart and stimulate the heart with the pulses generated in pacemaker. Battery and generators are inside a space titanium container which is placed inside the body.

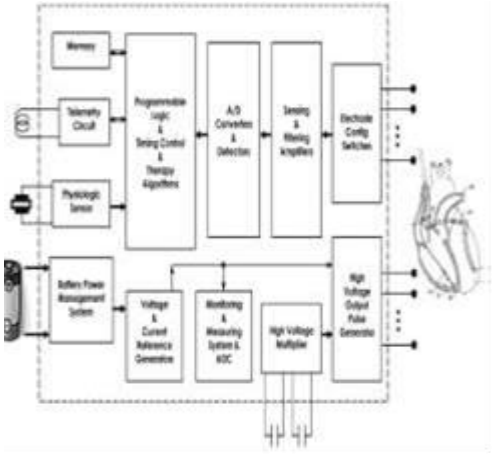

Fig. 1. Functional blocks of Peace Maker

### 3. Successive approximation ADC

This section describes different components of SAR ADC architecture. The main components of SAR ADC are Sample and Hold, a Digital to Analog Converter (DAC), a Comparator and a SAR Logic.

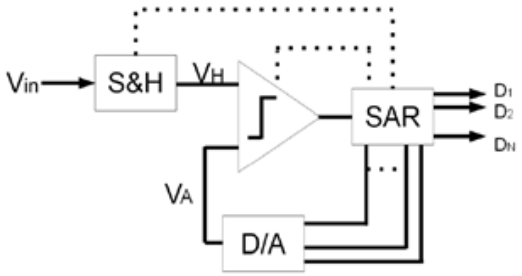


Fig. 2. Sample and Hold

#### A. *Operational amplifier*

The main building block of analog circuit design is the operational amplifier (op amp).Its primary use is to provide sufficient gain and to implement all analog signal processing functions using negative feedback .Such analog signal processing functions include amplification, integration, filtering and summation .Op-amps with vastly different level of complexity are used to realize functions ranging from dc bias generation to high gain amplification and filtering or ADC's.

#### B. *Sample and hold*

The sample and hold uses a capacitor and an analog switch to connect or isolate the capacitor from the input. An operational amplifier connected as follower avoids the effects of the load. The amplifier can be powered down in order to reduce the power consumption when the circuit is in the standby mode. The most basic form of sample and hold circuit combines a switch and a capacitor, the operation of the circuit as follows. In sampling mode the switch is "on", creating the signal path that allows the capacitor to track an input voltage .When the switch is "off" an open circuit is created that isolates the capacitor from the input, hence changing the circuit from sampling mode into holding mode.

#### C. *Comparator*

The comparator is an essential part in the SAR ADC to perform the binary search algorithm .Comparator in the SAR ADC takes more power consumption than other blocks .A comparator generates a logic output high or low based on the comparison of the analog input with a reference voltage. In an ideal comparator with infinite gain for input voltages higher than reference voltage, the comparator outputs logical one and for the input voltages lower than the reference voltage it produces zero at the output. In this architecture two inverters are inserted between the two stages of the conventional two-stage dynamic latched comparator in order to strengthen the voltage signal at DI nodes providing higher regeneration speed in addition to the advantage of convention two-stage dynamic latched comparator such as power efficiency high speed, and low kickback noise and lower input –referred offset. In the reset phase when clock signal is low, PMOS transistors in the gain stage are on and charge the capacitances of Di nodes to VDD and subsequently the Di' nodes are discharged to ground, thus, there is no static path and no static power dissipation during reset phase. The Di' nodes are discharged to ground and the PMOS transistors of the regeneration stage turn on and charge the output nodes as well as regenerative nodes i.e. drain of the NMOS transistors to VDD. During evaluation phase when clock signal turns to high, the Di nodes discharge through input and tail transistors to the ground with different rate, depending on the input voltage. While Di nodes are discharged, Di' nodes start to charge from 0 to VDD with different rate. Once either of Di' nodes reaches Vth, the NMOS transistor in the second stage is switched on, then the other transistor is also turned on. As a result, latch is activated and regenerates the digital voltage at the output from the small $\Delta V_{Di}$'.

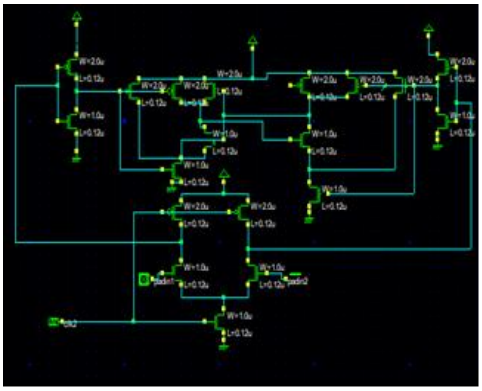

Fig. 2. Design of comparator

#### D. *Digital to analog converter*

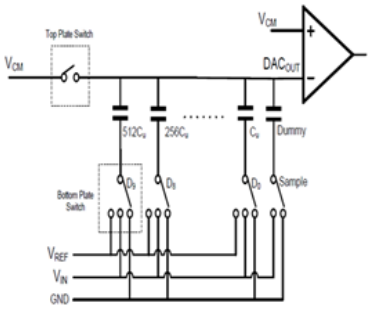


Fig. 3. DAC block diagram

The digital to analog converter has a resolution of 12 bits. The converter has been divided into three 4 bits D/A converters to reduce the total area. Each block can be powered down independently to reduce the power consumption. In this architecture we are using R-2R ladder network DAC .The advantage of the R-2R ladder method is only two values of resistors are used greatly simplifying the matching or trimming and temperature tracking .Since the output of the R-2R DAC is the product of the reference voltage and digital input word, the

R-2R ladder DAC is often called as MDAC. In this a 10-bit charge-redistribution back with BWC array was implemented in 65nm CMOS process. The fig. 3, shows the block diagram of the 10-bit DAC.

### *E. SAR logic*

Successive approximation register (SAR) control logic determines each bit successfully. The SAR contains N bit for an N-bit ADC. There are three possibilities for each bit, it can be set to, 1", reset to, "0'' or keeps its value. In the first step MSB is set to "1'' and other bits are reset to "0'', the digital word is converted to the analog value through DAC. The analog signal at the output of the DAC is inserted to the input of the comparator and is compared to the sampled input. Based on the comparator result, the SAR controller defines the MSB value. If the input is higher than the output of the DAC, the MSB remains at, "1'',otherwise it is reset to,,0''.The rest of the bits are determined in the same manner .In the last cycle ,the converted digital word is stored. Therefore, an N-bit SAR ADC takes N+1 clock cycles to perform a conversion.

SAR ADC implements the binary search algorithms using SAR control logic. In general, there are mainly two fundamental different approaches to design the SAR logic. The first one which is proposed by Anderson consists of a ring counter and a shift register .At least 2N flip flops are employed in this kind of SAR .The other ,which is proposed by Rossi ,contains N flip flops and some combinational logic. SAR architecture is commonly used in SAR ADC's due to its straightforward designed technique. This control logic encompasses a ring counter and a code register, the ring counter is in fact a shift register. For each conversion in clock cycle 0, the EOC signal is high and all Flip Flops outputs are reset to 0, and for the rest of cycle is low in the next clock cycle, the most Flip Flop is set to one which corresponds to MSB of the digital word to the DAC. Then the counter shifts '1' through the Flip Flops from MSB to LSB.

## 4. Experimental results

### *A. Operational amplifier*

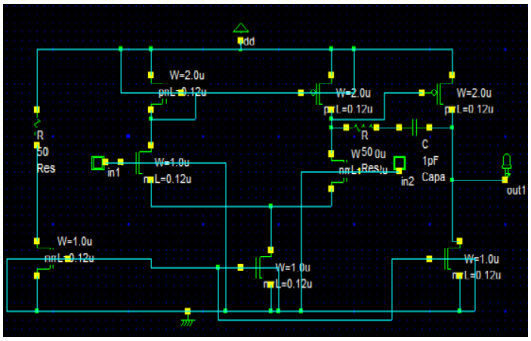


Fig. 4. Design of op amp

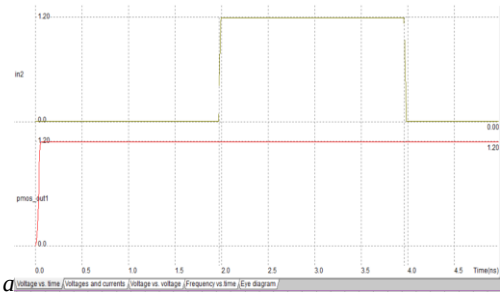


Fig. 5. Waveforms of op-amp (V vs. T)

### *B. Waveforms of OP-AMP (frequency vs. time)*

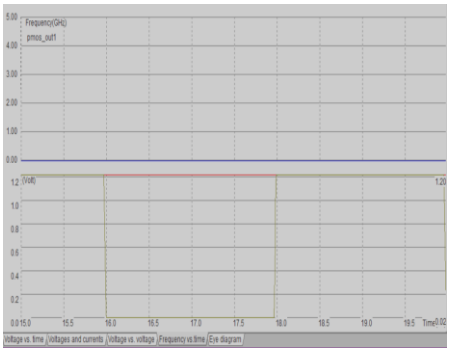


Fig. 6. Waveforms of op-amp (F vs. T)

## 5. Conclusion

This paper presents a 10-bit SAR ADC operating at 1kS/s and supply voltage of 1 V in 65nm CMOS technology. The power consumption of 12.4nW is achieved. The ADC employs a charge-redistribution DAC, a dynamic two-stage comparator, and a SAR control logic containing a sequencer and a ring counter. The ADC exhibits good performance and achieves an FOM of 14.7fJ/conversion-step with ENOB of 9.72 bit and SAR logic consumes the lowest power of 1.2nW at 1kS/s. Thus the power consumption of the SAR control logic is significantly reduced and consumes only %12 of the total power.

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