9-Level Trinity DC Source Inverter using Embedded Controller

R. Sreenivasan[1], M. Muthukumaran[2]

[1,2]*Assistant Professor, Department of EEE, CK College of Engineering and Technology, Cuddalore, India*

Abstract: **Trinary DC source cascaded H-bridge multilevel inverter and the switching pattern scheme is used to improve the performance of Multilevel Inverter (MLI) which reduces the switching losses. The proposed MLI can synthesize high quality output voltage near to sinusoidal waves. This scheme significantly reduces the Total Harmonic Distortion (THD) and switching losses. The circuit configuration is simple and easy to control. For the developed technique simulations are carried out through MATLAB/SIMULINK**

Keywords: **Trinary DC Source, Multi Level Inverter, Embedded controller**

1. Introduction

Nowadays multilevel inverters are widely used in power systems. Improved harmonic characteristics and ability to handle high voltage and high power are the major factors for developing such type of inverters. Also multilevel inverters have low switching stresses and high flexibility. There are several topologies which are diode-clamped, flying-capacitor and cascaded H-bridge cell [1]-[5]. Among them cascaded H-bridge multilevel inverters are used due to merits such as minimum number of components, reliability and modularity so that switching losses are reduced. In the point of obtaining a sinusoidal output voltage wave multilevel inverters may increase the number of output voltage levels. However it will need more components which results in complexity and increase in cost. To minimize these drawbacks multilevel inverters employing cascaded transformers have been studied [6]-[8]. Owing to the Trinary characteristic of output voltage they can synthesize high quality output voltage near to sinusoidal waves. By using a cascaded transformer galvanic isolation between source and loads are obtained. However the transformer may decrease the power conversion efficiency, as well as the volume and cost will be increased. To alleviate these problems we propose a cascaded H-bridge multilevel inverter using Trinary DC input source without transformers [6] where the circuit topology is simple and easy to control. This paper presents a single phase Trinary DC source nine level inverter topology for investigation with embedded controller switching technique. Simulations are performed using MATLAB-SIMULINK.

2. Basic operation of multilevel inverter

Fig. 1 shows a circuit configuration of a cascaded H-bridge multilevel inverter employing Trinary DC source. The input voltage of a first bridge source will be three times that of the second bridge source. By using Vdc and 3Vdc which can produce nine output voltage levels such as: -4Vdc, -3Vdc, -2Vdc, -Vdc, 0, Vdc, 2Vdc, 3Vdc, 4Vdc. The lower inverter generates a fundamental output voltage with three levels and the upper inverter adds or subtracts one level from the fundamental wave to synthesize stepped waves. Here the final output voltage levels becomes the sum of each terminal voltage of H-bridge and it is given as

VOUT =VHB1 +VHB2

In the proposed circuit topology if n number of H-bridge module has independent DC sources in sequence of the power of 3 then the expected output voltage level is given as
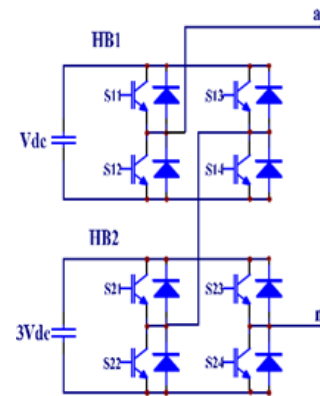
Vn=3n, where n=1, 2, 3…

Fig. 1. Trinary Source MLI

3. Stages of operation

A. *Stage 1: for 4VDC*

Switches on: S11, S14, S21, S24 and the remaining switches are in off condition, which produces 4Vdc.

B. *Stage 2: for 3VDC*

C. *Equations*

Switches on: S12, S14, S21, S24 and the remaining switches are in off condition, which produces 3Vdc.

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D. Stage 3: for 2VDC

Switches on: S12, S13, S21, S24 and the remaining switches are in off condition, which produces 2Vdc.

E. Stage 4: for 1VDC

Switches on: S11, S14, S22, S24 and the remaining switches are in off condition which produces 1Vdc.

F. Stage 5: for 0VDC

Switches on: S12, S14, S22, S24 and the remaining switches are in off condition, which produces 0Vdc.

G. Stage 6: for -1VDC

Switches on: S12, S13, S22, S24 and the remaining switches are in off condition, which produces -1Vdc.

H. Stage 7: for -2VDC

Switches on: S11, S14, S22, S23 and the remaining switches are in off condition, which produces -2Vdc.

I. Stage 8: for -3VDC

Switches on: S12, S14, S22, S23 and the remaining switches are in off condition, which produces -3Vdc.

J. Stage 9: for -4VDC

Switches on: S12, S13, S22, S23 and the remaining switches are in off condition, which produces -4Vdc.

Table 1
Switching sequence of trinary multi-level inverter

V_{out}	S11	S12	S13	S14	S21	S22	S23	S24
4Vdc	1	0	0	1	1	0	0	1
3Vdc	0	1	0	1	1	0	0	1
2Vdc	0	1	1	0	1	0	0	1
Vdc	1	0	0	1	0	1	0	1
0	0	1	0	1	0	1	0	1
-Vdc	0	1	1	0	0	1	0	1
-2Vdc	1	0	0	1	0	1	1	0
-3Vdc	0	1	0	1	0	1	1	0
-4Vdc	0	1	1	0	0	1	1	0

K. Trinary DC source

Fig1 shows a trinary dc source which contains cascaded H-bridge of two bridges (HB1 and HB2) having 1Vdc for first bridge and the second bridge is 3Vdc. The value of the voltage source of first bridge will be three times that of the second bridge to produce nine level inverter output. If the values of the voltage source in both the bridges are the same then it will produce 5-level inverter. If the value of the voltage source in first bridge will be twice that of the second bridge then it will produce 7-level inverter. It is compared with the conventional multilevel inverters i.e., diode-clamped, flying capacitor, cascaded H-bridge and cascaded transformer based multilevel inverter. The main drawback in diode-clamped is, it has a large number of clamping diodes where as in Flying capacitor method is, it has a lot of balancing capacitors.

L. Switching signal generation

Switching signal generation for proposed multilevel inverter

is generated using embedded controller. Fig. 2 to 9 shows the gating pattern generated using embedded controller
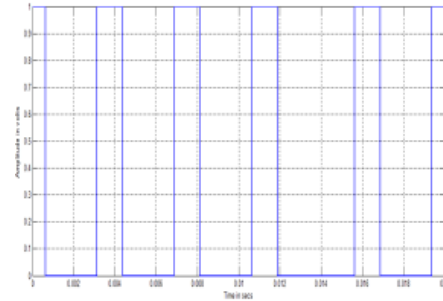

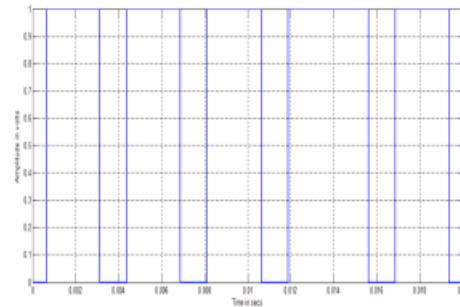Fig. 2. Gating pattern of Switch S11

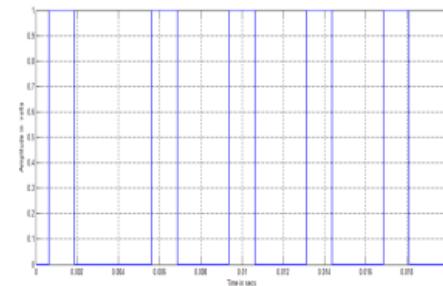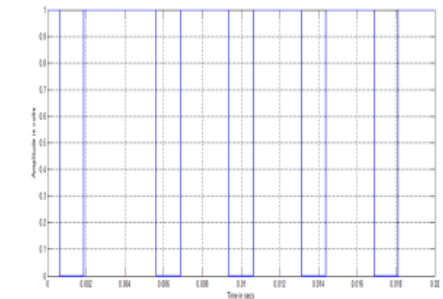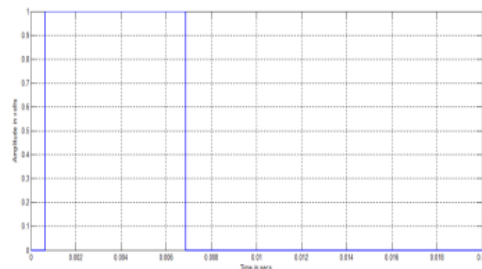Fig. 3. Gating pattern of Switch S12

Fig. 4. Gating pattern of Switch S13

Fig. 5. Gating pattern of Switch S14

Fig. 6. Gating pattern of Switch S21

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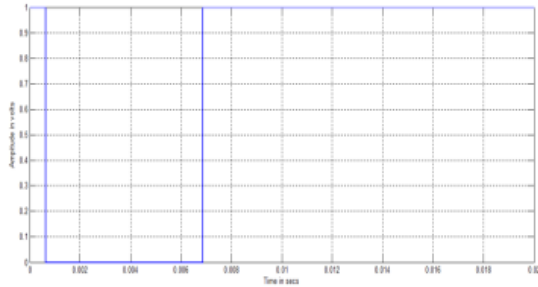**www.ijresm.com | ISSN (Online): 2581-5792**

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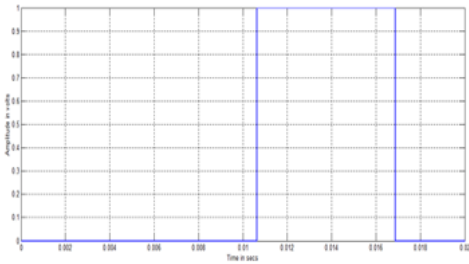Fig. 7. Gating pattern of Switch S22
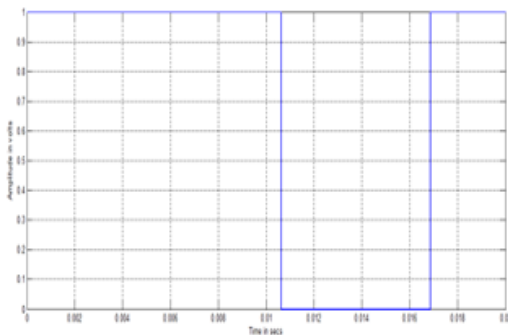

Fig. 8. Gating pattern of Switch S23

Fig. 9. Gating pattern of Switch S24

4. Simulations and results

The simulations are implemented using MATLAB. We can notice that the lower inverter generates a fundamental output voltage of three levels and the upper inverter adds or subtracts one level from the fundamental wave to synthesize stepped waves. Fig13 shows the FFT plot for nine level inverter. The final output voltage becomes the sum of terminal voltage of H-bridge modules. The following parameter values are used for simulation:
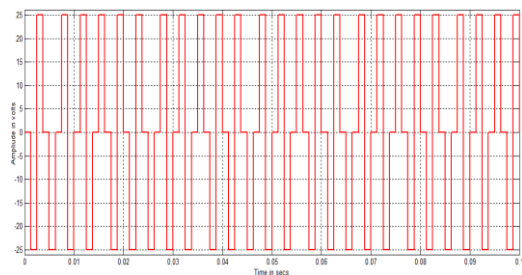
Vdc =25V, R (load) = 100 Ω.
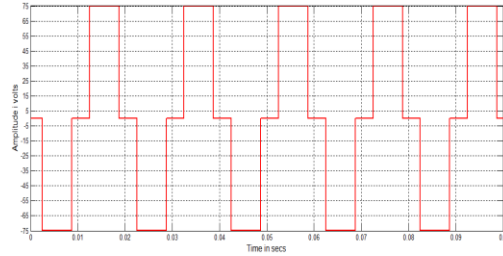

Fig. 10. Upper inverter terminal voltage

Fig. 11. Lower inverter terminal voltage
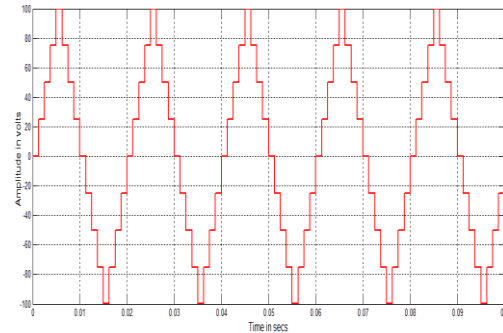

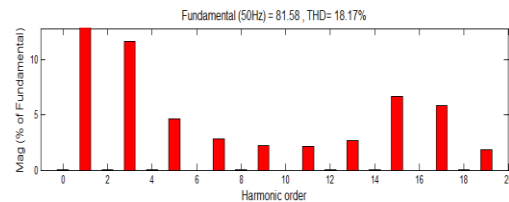Fig. 12. Nine level output voltage of trinary multi-level inverter

Fig. 13. FFT plot for nine level output voltages

5. Conclusion

Thus it is proposed that cascaded H-bridge multilevel inverter employing Trinary DC sources will obtain a large number of output voltage levels with minimum devices and synthesize high quality output voltage near to sinusoidal waves. Also in this paper embedded switching scheme is employed and the advantage of using digital scheme is that it reduces the uneven degradation of power switches and switching losses. It is observed that proposed topology produce THD of 18.17% which eliminates the complexity of generating gate signals when the stages are added. Valuable and presentable merits of the proposed approach are summarized as

- Economical circuit configuration to produce multilevel outputs by using Trinary input sources.
- Easy to increase of the output voltage levels and output power owing to modularity characteristic
- Little transition loss of switches due to
- low switching frequency and reduced EMI which is suitable for high voltage applications.

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