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Multiple-Input Floating Gate MOS Transistor Based Differential Pair Design

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***Abstract*—Analysis of Floating Gate MOSFETs (FGMOS) is carried out. Multiple-Input FGMOS differential amplifier with low threshold voltage is presented. The new differential amplifier structure whose output goes rail-to-rail operating with low supply voltage (± 1.65 V) is proposed. Results of circuit simulations in HSPICE using the simulation model of MIFGMOS transistor have been shown.**

***Index Terms*—Floating-Gate MOSFETs, Low-voltage, Analog Circuits, HSPICE.**

I. Introduction

Differential amplifiers are widely used as input stages in the design of operational amplifiers, OTAs, comparators and mixers. Fig. 1 shows a simple NMOS differential pair. It is biased by a single saturated NMOS transistor which provides a constant current source. The sum of two output currents, I_1+I_2 is kept constant at fixed value of I_B, to maintain constant transconductance.

The voltage on a common source node moves up and down along with the input voltages V_1 and V_2.

To keep up a constant trans conductance for such a differential pair, the common-mode input voltage must be greater than ground. As a result of this, the gate-to-source voltage of input transistor is large enough to pass a significant amount of current I_B and the transistor responsible for sinking bias current remains in saturation. The input common-mode voltage should be larger than V_{TO}+V_{SAT} for bias currents at or within the close range of threshold value.

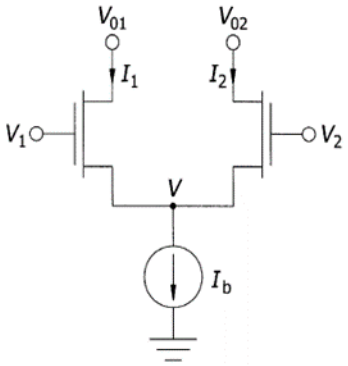

Fig. 1. Basic differential pair

This constraint on the common-mode input voltage makes the conventional differential pair unattractive for low-voltage applications. To overcome this limitation of simple differential pair in low voltage applications, differential pair is constructed from floating-gate MOS transistors. Charge deposited on the gates of FGMOS transistors are used as a level shift in such a way that common-mode control input gate voltage will be at ground while the common-mode floating gate voltage is high enough to enable proper operation of the differential pair.

II. Floating-Gate Mosfets

Floating-gate MOS transistors are widely used in reprogrammable memory systems. Fig. 2 describes physical layout, schematic symbol and equivalent circuit of MIFG MOS transistor. Until recently, the floating gate transistors had only been used in digital electronics EEPROM devices.

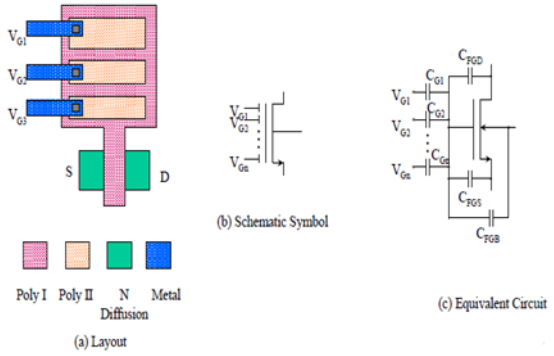

Fig. 2. Layout, schematic symbol and equivalent circuit of MIFG MOS transistor

The voltage on floating gate V_{FG} can be given by:

$$V_{FG} = \sum_{i=1}^{N} \frac{C_i}{C_T} V_i + \frac{C_{GS}}{C_T} V_S + \frac{C_{GD}}{C_T} V_D + \frac{Q_{FG}}{C_T} \quad (1)$$

C_i is the set of capacitors associated with effective inputs and the floating gate.

C_T = C_1+ C_2+ C_{FGS}+ C_{FGB}+ C_{FGD} is the total floating gate capacitance.

MIFG MOSFET has proved a great success in the field of VLSI. Many researchers have reported that it offers an alternative solution for circuit designers to build efficient low voltage circuits with reduced power supply restriction by adjusting the transistor threshold voltage. The threshold voltage

seen from the input gates can be modified by varying the amount of static charge on the floating gate by using ultra violet shining, hot-electron injection and Fowler-Nordheim process.

MIFG transistor circuits provides not only the easy implementation of linear weighted voltage addition and analog memory capabilities but also other useful features such as improvement in linearity with rail-to-rail swings and also low voltage operation. The circuit presented in this paper uses a folded cascade circuit design for low voltage applications.

A floating gate simulation model was proposed and it defines the coupling of the input capacitors as well as the parasitic capacitors as shown in Fig. 3.

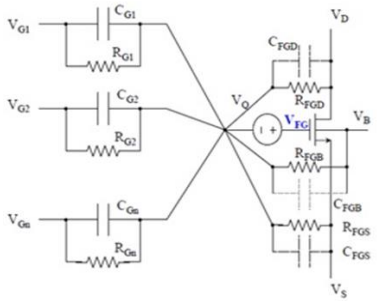

Fig. 3. MIFG MOS transistor simulation model

In order to solve the convergence problem and minimize the loading effect to the circuit, a resistor connected in parallel with each input capacitor is added to the model. Now, these resistors are selected in such manner so that every branch possesses the same time constant.

III. MIFG Differential Pair

There are two circuits proposed for differential amplifier. They are explained in the next section given below.

A. MIFG Differential Pair

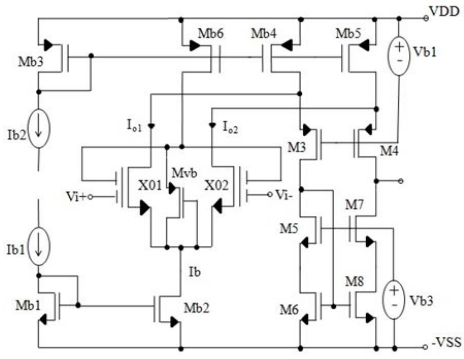

Fig. 4. MIFG MOS Differential Pair with low V_T

MIFG differential pair shown in Fig. 4 is a low threshold voltage (VT) transistor. The floating voltage source used in the circuit may limit its common mode swing range if the floating voltage source cannot swing out of the supply rails. Trans conductance of differential pair is attenuated due to floating gate. The major drawback of this differential pair is that it cannot have rail-to-rail range.

B. Rail -to-Rail MIFG Differential Pair

To make a differential amplifier work under any circumstances, a differential input with rail-to-rail common mode range is required. The variation in transconductance of input stage is not desirable because it prevents the optimal frequency compensation of the amplifier. There are other drawbacks of changing transconductance of the differential pair. For instance, g_m variation may introduce extra harmonic distortion because of the changing voltage gain.

The new rail-to-rail MIFG MOS Differential pair structure is biased using a non-floating voltage source and folded cascode circuit is used in low voltage input stage.

Almost, constant transconductance is achieved using the improved circuit shown in Fig. 5.

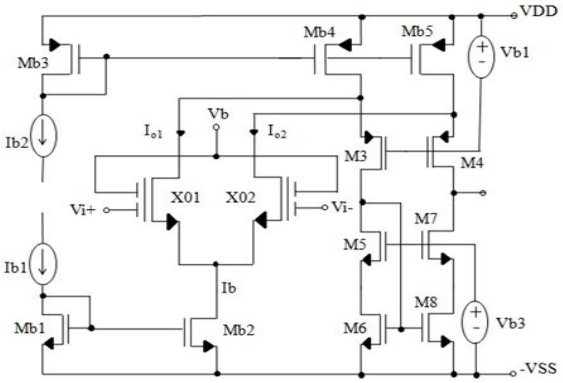

Fig. 5. Rail-to-Rail MIFG MOS differential pair

The voltage V_F on 2-input floating gate transistors can be given as:

$$V_F = w_0V_0 + w_1V_1 + w_2V_2 \quad (2)$$

where, $w_i = {}^{C_i}/_{C_{TOTAL}}$, i=0,1,2

Normally, C_i (i = 1, 2) is much larger than C_0, which means w_0 is very small. Thus, we can reach the approximation: $w_1 + w_2 = 1$.

When V_{icm} (common mode input voltage) is almost equal to V_{DD}, for N type transistor, the floating gate can be at V_{DD} as long as the voltage at drain of the transistor is greater than V_{DD}-V_{TN}. Thus, V_b can be directly V_{DD}.

When V_{icm} is close to the negative rail supply, there is a probability that tail current transistor may have no room to operate in saturation region.

So, we must increase the voltage on common mode node of the floating gate $V_{FG,cm}$.

$$V_{FG,cm} = w_1V_{icm} + w_2V_b \quad (3)$$

Due to this, we must have high bias voltage V_b, which takes the maximum value of V_{DD}. When $V_b = V_{DD}$ and $V_{icm} = -V_{SS}$,

the above equation can be written as

$$V_{FG,cm} = -w_1 V_{SS} + w_2 V_{DD} = -w_1 V_{SS} + (1 - w_1) V_{DD} = V_{DD} - w_1 (V_{SS} + V_{DD}) \quad (4)$$

For the proper operation of M1, M2 and tail current transistor, the given inequality should be satisfied:

$$V_{FG,cm} \geq -V_{SS} + \left(V_{GS,M1,M2} + V_{DSAT,MTAIL}\right) \quad (5)$$

From the above equations, we have

$$(V_{DD} + V_{SS}) \geq \left(V_{GS,M1M2} + V_{DSAT,MTAIL}\right) / (1 - w_1) \quad (6)$$

Therefore, minimum supply voltage is

$$V_{sup} = \left(V_{GS,M1,M2} + V_{DSAT,MTAIL}\right) / (1 - w_1) \quad (7)$$

IV. Simulation Results

The simulation results of proposed multiple-input floating gate MOS transistor based differential pair using TSMC 0.18µm CMOS process technology parameters in HSPICE is obtained. By following the common design procedure and considering the specified performance and model parameters, the sizes of the transistors are determined.

The input-output transfer characteristic curve of the proposed differential pair is shown in Fig. 6. The output voltage swing is observed to be rail-to-rail in DC. But it is also found that the transconductance parameter is degraded and this will ultimately result in lower gain.

The frequency response of the designed MIFG MOS differential pair is shown in Fig. 7. In the test setup, a differential AC signal is given to the inputs along with the DC bias potential is also applied. Through AC response, we can simulate the schematic to find out the bode plot.

It can be seen that the open loop gain is 45.008 dB for MIFG differential pair with -3 dB frequency of 2MHz. AC analysis is used to obtain CMRR of MIFG based MOS differential pair. CMRR is found to be 66 dB.

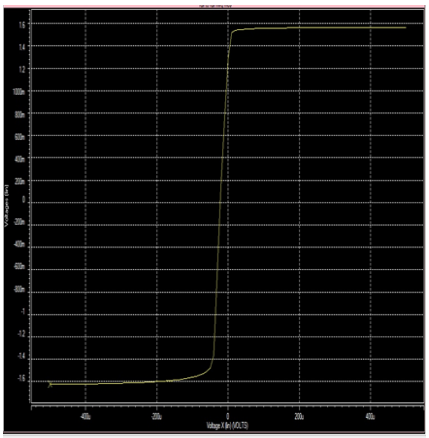

Fig. 6. DC Input-Output Transfer Characteristics of the MIFG MOS diffferential pair

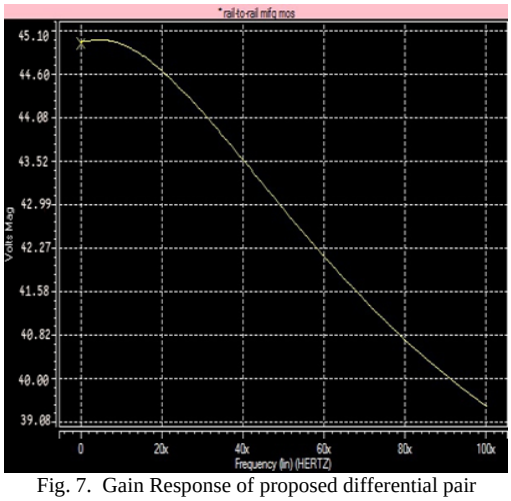

Fig. 7. Gain Response of proposed differential pair

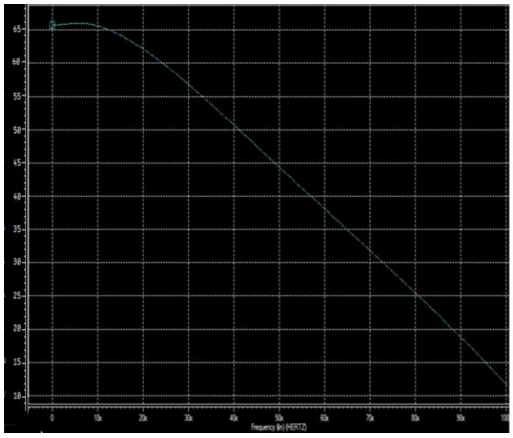

Fig. 8. CMRR of proposed differential pair

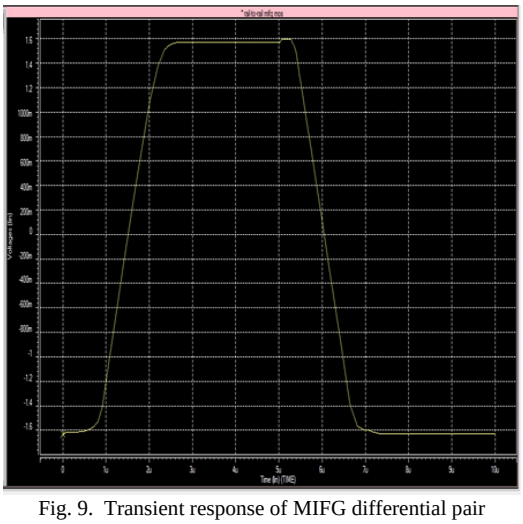

Fig. 9. Transient response of MIFG differential pair

The transient response of proposed differential pair is shown in Fig. 9. It has output voltage swing from -1.5 volts to 1.5 volts. It is obtained by applying pulse input waveform.

The positive slew rate estimated in Fig. 9 is found to be +2.2 Volts/µsec and negative slew rate is found to be −2.3 Volts/µsec.

The value of offset voltage is determined by dc analysis and is found to be 0.61 micro volts.

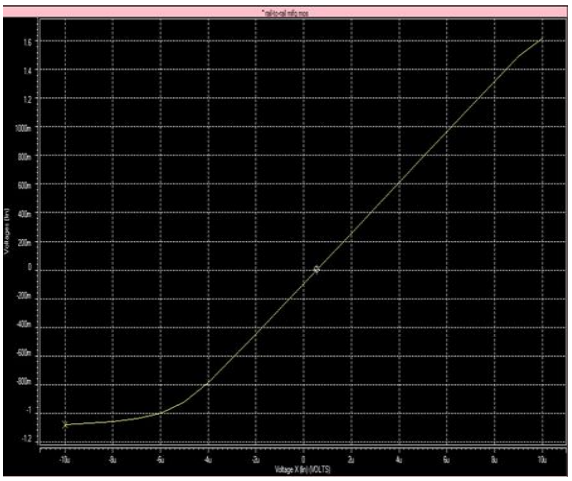

Fig. 10. Offset voltage measurement of MIFG MOS differential pair

V. Conclusion

In this paper, a low power and low offset voltage differential amplifier is presented. This differential pair offers rail-to-rail output voltage swing and hence can be used for any operational amplifier configuration. The major drawback of this MIFG differential pair is that transconductance value is degraded and hence smaller gain and gain bandwidth product is observed. The simulation is done in HSPICE 180nm technology with ±1.65 V power supply and dc bias current of 20µA.

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