International Journal of Research in Engineering, Science and Management
Volume-1, Issue-10, October-2018
www.ijresm.com | ISSN (Online): 2581-5782

Smart Memory

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***Abstract*—A smart memories chip is made up of many processing files, each processing files contains Local Memory, Local Interconnect, and a Processor Core. For efficiency of smart memories in computation under a wide class of possible application, the memories, the wires and the computational model can all be altered to match the all applications used in this process. To show the applicability of this design, two different machine is implemented in the opposite end of the architectural spectrum, imagine stream processor and the Hydra Speculative Multiprocessor will mapped onto Smart Memories Computing subsite. It is successfully map these architectures with only modest performance degradation.**

***Index Terms*—Smart Memories, Memory System, Processor, I/O bandwidth**

I. Introduction

The continued scaling of integrated circuit fabrication technology will dramatically affect the architecture of future computing systems. Scaling will makes computation cheaper, smaller and lower power, thus enabling more sophisticated computation in a growing number of embedded computation. This spreads Wireless communication devices, gaming consoles, and handled PDAs. These new application have different characteristics from today's standards workloads, often containing highly data-Parallel streaming behaviour.

A. Smart memories overview

- At the highest level, a Smart Memories chip is a modular computer. It contains an array of processor titles and on-die DRAM memories connected by a packet-based, Dynamically-routed network.
- The network also connects to high-speed links on the pins of the chips to allow

Construction of multi-chip systems. Most of the initial hardware design works in the Smart Memories.

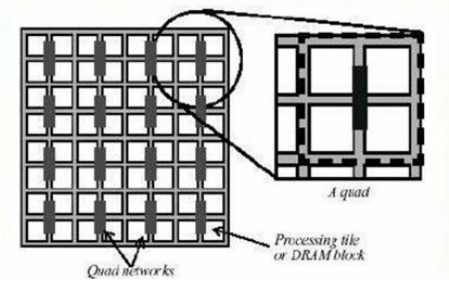

Fig. 1. Quad networks

II. Memory System

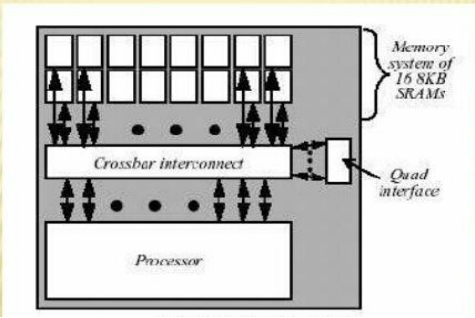

Fig. 2. Memory system

Interconnect

To connect the different memory mats to desired processor or quad interface port, the tile contains a dynamically routed crossbar, which supports up to 8 concurrent references.

Processor

- The processor portion of a Smart Memories tile is a 64-bit processing engine with Reconfigurable instruction format/decode. The computation resources of the Tile consist of two integer clusters and one floating point (FP) cluster. The Arrangement of these units and the FP clusters unit mix.
- Each integer cluster consists of an ALU, register file, and load/store unit. I/O Technology Choice in Smart Memory.
- Smart Memory reduce the chip I/O bandwidth significantly.

Advantages

- Reduced chip I/O bandwidth
- High performance and low latency
- Feature rich, flexible and programmable
- Lower cost
- One chip for several functions

Disadvantages

Packet Processing Bottlenecks

- Date away from compute
- I/O and memory bandwidth

Smart Memory

- Keep compute close to data
- Keep locking close to data
- Provide inter-memory connect

III. Conclusion

Smart Memories addresses the issue by extending the notion of a program. In conventional computing systems the memories and interconnect between the processors and memories is fixed, and what the programmer modifies is the code that runs on the processor. While the model is completely general, for many application it is not very efficient. In Smart Memories, the user can program the wires and the memory, as well as the processors.

References

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