Bit Transition Identifier (BTI) for Low Power TPGs

V. M. Thoulath Begam

Professor, Department of ECE, A.R. College of Engineering & Technology, Tirunelveli, India

Abstract—**Power dissipation is the major problem in testing VLSI circuits. The application of random test input patterns causes high switching activity that increases dynamic power dissipation. The proposed Bit Transition Identifier (BTI) identifies the consecutive test patterns that have more transitions. It contains an XOR network with a modified adder circuit. Adder finds the number of transitions. BTI was implemented with different adders and the results show that the proposed BTI identifies more transition patterns with less delay.**

Index Terms—**bit transition, low power testing, switching activity, test pattern generator**

I. INTRODUCTION

In VLSI technology a single integrated chip contains a very large number of transistors. Testing the chip functionality is extremely complex and very time consuming. Cost of detecting a fault at board level is nearly 10 times higher than that at the chip level. In test mode the power dissipation is 200% more than that in the normal mode. Because of this high power dissipation battery life is shortened.

Another important issue with high power consumption is the rise in temperature. If the temperature rises above a threshold value the Integrated Circuit may be damaged in some of the circuits and the circuit functionality may also change as a result of high temperatures above the threshold level. Another parameter that is affected by high power consumption is yield loss. Due to high temperature traditional cooling techniques may not be sufficient. Therefore expensive cooling techniques are to be used and that in turn will increase the cost of the IC. Further, the area occupied may also affect the yield loss. Because of the excessive test power, heat dissipation also will also be increased. In order to handle high temperature effective packaging is required.

Integrated circuits and systems have been tested using a pseudorandom Built-in Self-Test (BIST) generator which generates test inputs. For circuits with hard-to-detect faults, a large number of random patterns have to be generated to achieve high fault coverage. These random test patterns are less correlative which increases the dynamic power dissipation. Dynamic power dissipation is proportional to switching activity of the circuit and it is the dominant factor in the total power dissipation of the circuit. For technologies up to 0.35 μm, the dynamic dissipation is about 80% of a circuit's total dissipation.

As the technology scales down, i.e. submicron technologies, its contribution decreases but still remains the dominant factor. Reducing power consumption in test mode is an important objective in circuit design.

Many low power testing methods for VLSI circuits have been proposed. They mainly deal with the reduction of switching transitions between the consecutive test patterns by inserting test vectors between all consecutive test patterns. This increases the correlation between them and reduces power dissipation. Unnecessary insertion of test vectors between all consecutive test patterns (sometimes) increase switching transitions and test time. But Transition Counters (BTC) increase area and delay. The proposed BTI identifies more transition patterns with less delay. Test vectors can be inserted only in between these patterns which reduces power dissipation and test time.

The layout of the paper is as follows. In section 2, discusses low power testing methods. Section 3 explains the implementation of BTI with low power Test Pattern Generator (TPG). The proposed BTI and the new adder designs are explained in section 4. Experimental results and conclusions are presented in sections 5 and 6 respectively.

II. LOW POWER TESTING METHODS

Switching activity is defined as the rate of switching of the circuit from '0' to '1' and '1' to '0' while operating in the circuit. This switching is taken into consideration whenever bus power consumption is calculated. Switching activity can be determined by calculating the number of bit transitions takes place during actual operation of logic in circuit. By minimizing the switching activity, the average dynamic power consumption on bus can be reduced as it is directly proportional to switching activity factor. For some tests it is possible to find the switching activity such that it would not exceed that possible during functional operation [2]. Transition Density [8] which is average number of transitions per second at a circuit node is a measure of switching activity. Generally switching activity occurs at node and difficult to evaluate, estimation model are given in [3]. Transition Density [8] which is average number of transitions per second at a circuit node is a measure of switching activity. Generally switching activity occurs at node and difficult to evaluate, estimation model are given in [3]. A lot of research work is going on to reduce dynamic power consumption on bus by reducing the switching activity [9]. Low

International Journal of Research in Engineering, Science and Management
Volume-1, Issue-10, October-2018
www.ijresm.com | ISSN (Online): 2581-5782

73

power address generators are proposed in [10, 1], which mainly focus on reducing switching activity. Research works are going on reducing power through charging and discharging of node capacitance. Based on SBST techniques for optimizing and other key aspects a software-based self-testing [5] was proposed in the microprocessor test and validation process. The low transition test vectors inserted between each consecutive pattern, increasing testing time was also reported in LT-LFSR [6]. But it has negligible effect on the fault coverage convergence. LFSR characteristic polynomial plays an important role in test pattern generation. Both testing time and fault coverage also depend on polynomial equation. The polynomial based method [7] addresses the problem of computing a polynomial of small degree directly from the given test set without having to solve multiple non-linear systems and fixing a priori the polynomial degree. Higher levels of integration and shrinking line widths have led to a generation of devices which are more sensitive to power dissipation and reliability problems [12]. The paper [6] explains reducing power through charging and discharging of node capacitance. A bit transition counter [4] calculates the number of transitions takes place while applying the test patterns by these TPG's. It also can be used in address generators. BTC uses different counters which increases area. But in the proposed design high transition patterns are identified using a simple adder.

III. Implementation of Bit Transition Identifier

The existing designs count the number transitions in consecutive patterns which increase area and static power. But identifying the more transition patterns is enough for test vector insertion method. The proposed design only identifies the more transition patterns.
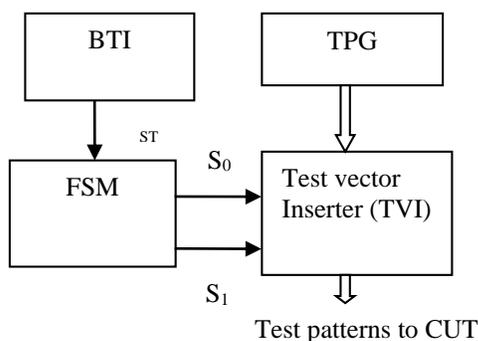

Fig. 1. Implementation of BTI in low power TPG

As shown in Fig.1 TPG generates random patterns. TVI inserts test vectors in between the patterns. If BTI is included in this arrangement, it finds high transition patterns and only in between them test vectors can be inserted.

Before designing Bit Transition Identifier (BTI), first we decide the requirements of BTI with what it should be designed. Here first the transition between each successive bit in the consecutive patterns should be found and then the total number of transitions should be identified. Considering the above points in considerations the BTI is designed which is capable of identifying the number of bit transitions in the successive patterns. For example if data changes from "11110010" to "11100101" the bit transitions are 4 as transitions takes place at bit(4), bit(2), bit(1) and bit(0). The number of transitions cannot exceed the total number of bits. The BTI should be capable of counting number of transitions at every transition between successive test pattern.

IV. Design of Bit Transition Identifier

Bit Transition Identifier is constructed by using (N-1) number of XOR gates (N is the number of bits in test pattern), the proposed adder circuit and an OR gate. XOR gates are used to check the transition between vertical bits. Fig. 2 shows BTI for an 8-bit test pattern.
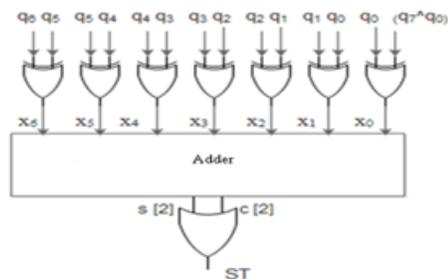

Fig. 2. The proposed Bit Transition Identifier

Present and next test pattern bits are applied as inputs to XOR gates. If test bits are not same, then the XOR gate's output is 1. These 1's are added using the proposed adder. More numbers of 1's are indicated by $(N-1)^{th}$ bit of sum and carry output of adder. The required sum and carry outputs which indicate more number of 1's only given to OR gate inputs to produce ST output. The output of BTI is '1' if the test patterns are having more transitions.

Depending on the requirement OR gate inputs can be changed. By changing the inputs of the OR gate, test patterns with different number of transition can be identified. The proposed design identifies consecutive patterns (8-bit) that have more than 3 transitions.

A. The Proposed Adder
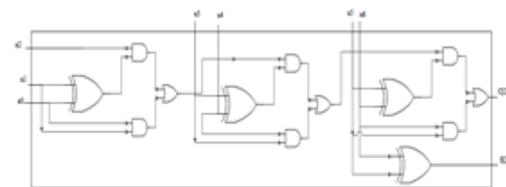
Fig. 3. The proposed adder

The proposed adder design is shown in Fig. 3. The XOR outputs (x_0-x_6) are added using an 8-bit proposed adder. To reduce more power dissipation the inputs of OR gates can be varied. The OR gate output is applied to FSM as input. The

74

International Journal of Research in Engineering, Science and Management
Volume-1, Issue-10, October-2018
www.ijresm.com | ISSN (Online): 2581-5782

number of bits in the TP or the number inputs of CUT. By observing the final bit of sum and carry, high transition patterns can be identified. Therefore other sum generators are not needed in this adder. The proposed adder has been constructed using all carry generators with final sum bit generator. Therefore BTI has less delay and small area.

V. Experimental Results

The BTI is designed in Verilog. The simulation of the Verilog code is performed in Xilinx software and the waveforms are shown in Fig. 4.
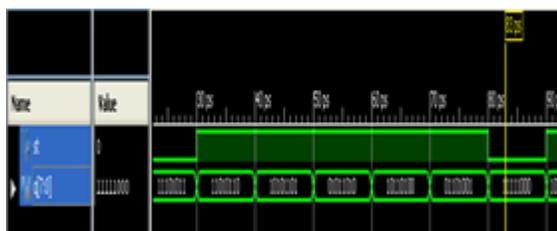
Fig. 4. Simulation output of Bit Transition Identifier

The Pattern "11010110" has more transitions and it is indentified by BTI as the output "st" is high. The pattern "11111000" has few bit transitions. The BTI output for this pattern is low. The output of TPG is indicated by 'st'. The proposed BTI identifies the patterns that have more than 3 bit transitions.

TABLE I
BTI IMPLEMENTATION WITH DIFFERENT TYPE OF ADDERS

Device utilization summary	The proposed adder	carry save adder	CLA	carry skip adder
No. of Slices (out of 2448)	1	5	4	5
No. of 4 I/P LUTs (out of 4896)	2	9	8	9
No. of IOs:	8	14	14	14
No. of bonded IOBs: (out of 158)	8 (5%)	14 (8%)	14 (8%)	14 (8%)
Total Delay (ns)	7.030	7.916	8.959	7.930

The Table I shows the number of devices utilized by BTI when it is implemented using different adders. Codes for BTI synthesized with different adders and the results were observed from the synthesis report. The proposed adder has less delay and uses fewer devices. From Table I it is proved that BTI using the proposed adder needs few devices and has less total delay.

VI. Conclusion

In this paper a simple Bit Transition Identifier is designed and implemented on LFSR –TPG for digital circuit testing. It identifies more transitions patterns and helpful in reducing dynamic power dissipation in TPGs without increasing the test time. This design can be implemented on any type of TPG and it needs few components with less delay.

References

[1] C.Ravishankar Reddy, Shaik Zilani, V.Sumalatha Low Power, Low-Transition Random Pattern Generator, proc. International Journal of Engineering Research & Technology 1(5), 2012, pp. 1-6.
[2] Irith Pomeranz and Sudhakar M. Reddy, Switching Activity as a Test Compaction Heuristic for Transition Faults, proc. Very Large Scale Integration (VLSI) Systems, IEEE Transactions on 18(9), 2010, pp. 1357-1361
[3] F. Najm, Transition Density: A New Measure of Activity in Digital Circuits, in IEEE Trans. On Computer- Aided Design of Integrated Circuits and Systems, 12(2), 1993.
[4] Amandeep Singh, Balwinder Singh, Design and Implementation of Bit Transition Counter, Circuits and Systems: An International Journal (CSIJ), Vol. 1, No. 1, January 2014, pp. 31-37.
[5] Mikhail Psarakis, 'Microprocessor Software-Based Self-Testing', IEEE Design & Test of Computers, vol. 27, no. 3, 2010, pp. 4-19.
[6] Ahmed, N, Nourani, M & Tehranipoor, M 2008, 'Low-transition test pattern generation for BIST-based applications', IEEE Transactions on Computers, vol. 57, no. 3, pp. 303–315.
[7] Haoqi Ren, Sch & Zhenya Xiong 2015, 'A Multi-polynomial LFSR Based BIST Pattern Generator for Pseudorandom Testing', Information Science and Control Engineering (ICISCE), 2015, 2nd International Conference, pp. 568–572.
[8] Yazdan Aghaghiri, Farzan Fallah and Massoud Pedram, ALBORZ: Address Level Bus Power Optimization, proc. International Symposium on Quality Electronic Design, 2002, pp. 470-475.
[9] Yazdan Aghaghiri, Farzan Fallah and Massoud Pedram, A class of Irredundant encoding techniques for reducing bus power, proc. Journal of Circuits, Systems and Computers,11, 2002, pp. 445-448.
[10] Ahmed N.Awad and Abdallatif S.Abu-Issa, Low Power Address Generator for Memory Built-In Self-Test, proc. The research bulletin of Jordan ACM, 2(3), 2011, pp. 52-56.
[11] K S Sainarayanan, C Raghunandan, J V R Ravindra and M B Srinivas, Bus Coding to Minimize Redundant Bit Transitions, proc. IEEE Region 10 Conference on TENCON , 2007, pp. 1-6.
[12] Farid N. Najm and Michael G.Xakellis, Statistical Estimation of the Swiching Activity in VLSI circuits, proc. VLSI Design, 7(3), 1998, pp. 243-254.